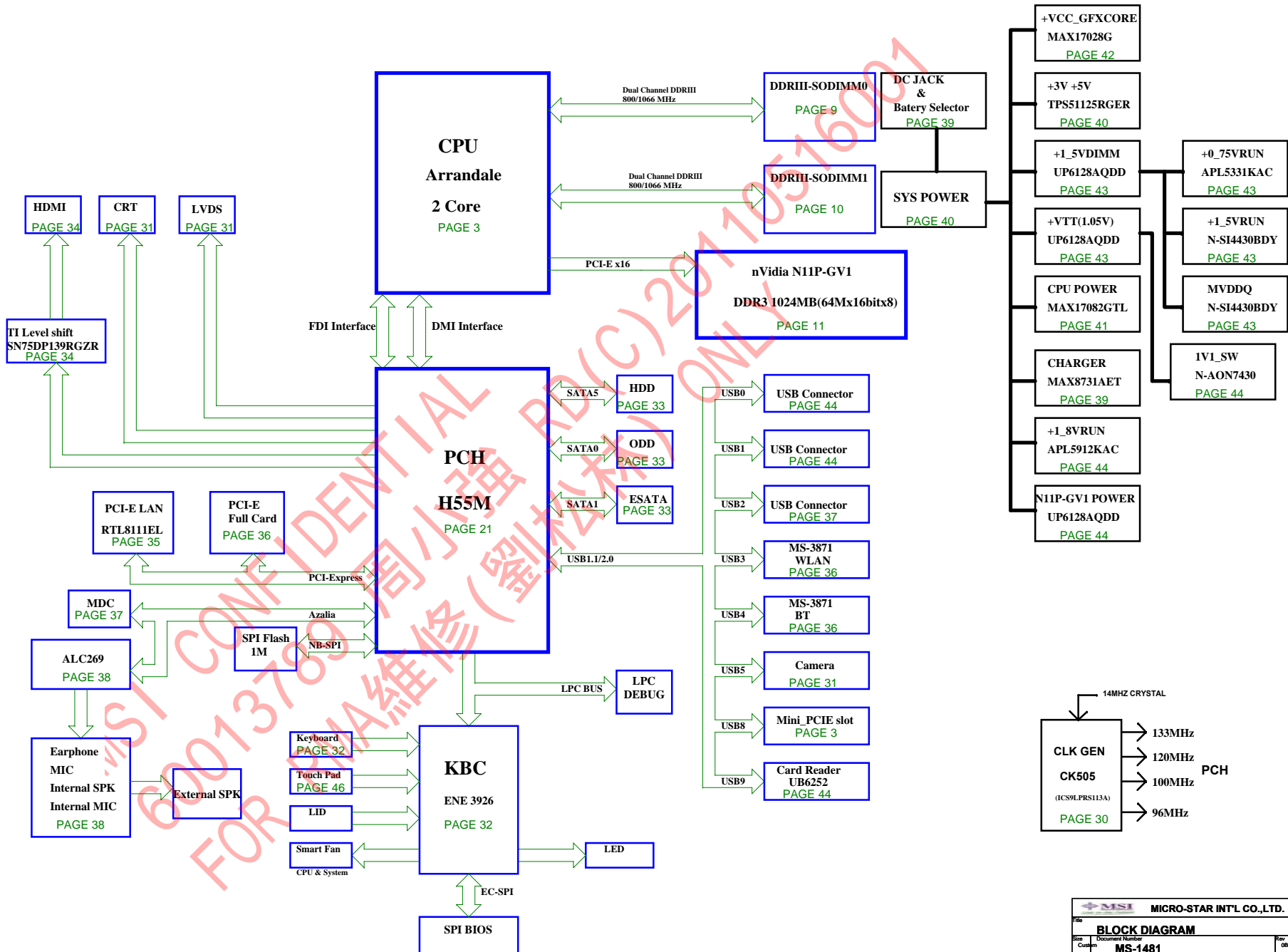


Release Date :2010/03/19

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30 : CLOCK GEN (ICS9LPRS113A)
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32 : KBC/EC/uP (KB3926)
33 : ODD, HDD, ESATA, LED, FAN
34 : HDMI & SWITCH
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36 : WLAN, BT, Combo, 3G SIM CARD
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38 : Audio ALC269
39 : M_Battery select & Charger
40 : M_System Power
41 : M_CPU power
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43 : M_SMDDR_VTERM /1_5VRUN
44 : M_VTT Power, +1.8VRUN, NVVDD
45 : 1481A_Card Reader, Audio, USB
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48 : Screw / ME
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

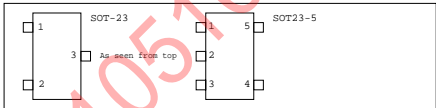
Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
PWR_SRC	19V	S0,(S3-S5)	
+5VALW	5V	S0,(S3-S5)	
+5VRUN	5V	S0	
+5VSUS	5V	S0	
+3VALW	3.3V	S0,(S3-S5)	
+3VSUS	3.3V	S0,(S3-S5)	LAN
+3VRUN	3.3V	S0	
+1_5VDIMM	1.5V	S0,S3	DDRIII core
+1_5VRUN	1.5V	S0	
VTT	1.05V	S0	PCH
+0_75VRUN	0.75V	S0	DDRIII command & control pull up.
+VCC_CORE	1.05V-1.1V	S0	CPU core rail
+VCC GFXCORE	1.1V	S0	Graphics core rail ( Dual Core only )
N11P_VDD_CORE	0.95V	S0	GPU core power
MVDDQ	1.5V	S0	GPU DDR3 power
1V1_SW	1.0V	S0	GPU PCIE power
+3VRUN_N11P	3.3V	S0	GPU I/O and DAC power

Net Naming Conventions

<b>Suffix</b>
F = Active Low Signal
<b>Prefix</b>
H = Host
M = DDR Memory
TP = Test Point (does not connect anywhere else)

PCB Footprints



AC Mode

Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF

Battery Mode

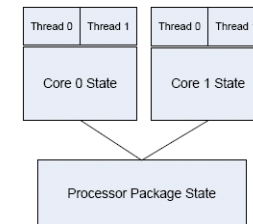
Power States	SLP_S3#	SLP_S4#	SLP_S5#	SLP_LAN#	+V*ALWAYS	+V*SUS	+V*RUN	CLK
S0 (Full on)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	HIGH	ON	OFF	OFF	OFF
S5 (Soft Off)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF

Westmere (formerly Nehalem-C) is the name given to the 32 nm die shrink of Nehalem.

Brand Name	Model (list)	L3 Cache size	Thermal Design Power
Intel Core i3	i3-3xxM	3 MB	35 W
Intel Core i5	i5-4xxM	3 MB	35 W
	i5-5xxM	3 MB	35 W
Intel Core i7	i7-6xxUM	4 MB	18 W
	i7-6xxLM	4 MB	25 W
	i7-6xxM	4 MB	35 W

The Core i3-3xx will be similar to the Core i5-4xx series but running at lower clock speeds and without Turbo Boost

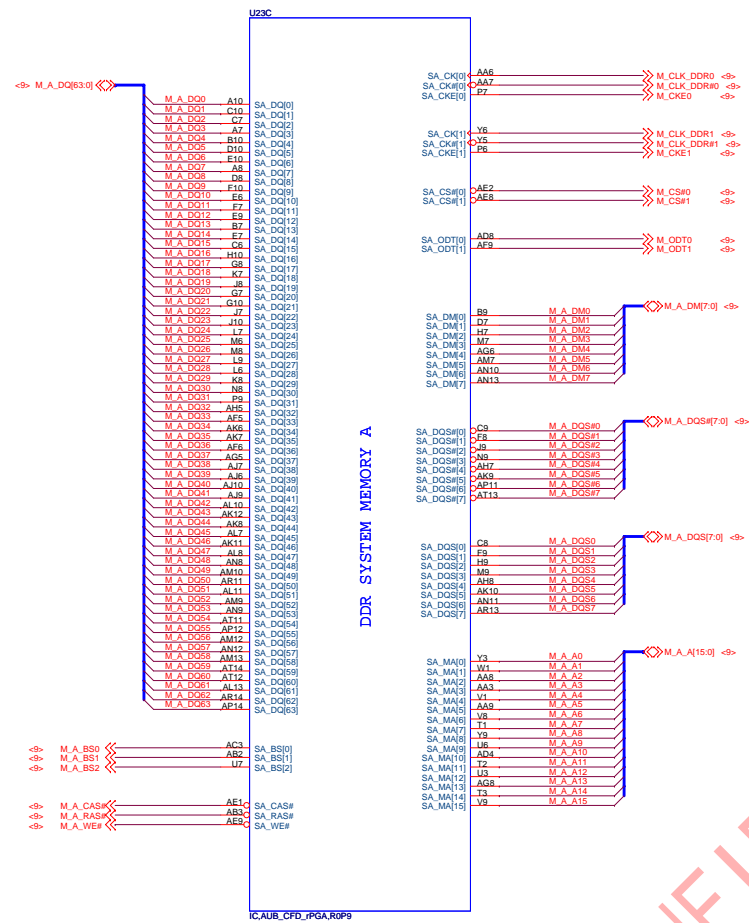
Brand	Intel Core i3			Intel Core i5		Intel Core i7		Intel Core i9	
Segment	POP1	POP2	POP3	ULV1	ULV2	LV1	LV2		
TDP	35W	35W	35W	18W	18W	25W	25W		
Cores / Threads	2/4	2/4	2/4	2/4	2/4	2/4	2/4		
CPU Base Freq (GHz)	2.40	2.53	2.66	1.06	1.2	2.00	2.13		
CPU Turbo Boost Technology Max 9C Turbo (GHz)	2.93	3.06	3.33	2.13	2.26	2.80	2.93		
DDR3 (MHz)	1066MHz	1066MHz	1066MHz	800MHz	800MHz	1066MHz	1066MHz		
L3 Cache	3MB	3MB	4MB	4MB	4MB	4MB	4MB		
Integrated Gfx	Yes	Yes	Yes	Yes	Yes	Yes	Yes		
Gfx Base Render Frequency	500MHz	500MHz	500MHz	166MHz	166MHz	266MHz	266MHz		
Intel® Turbo Boost Technology Max Gfx Freq (MHz)	766MHz	766MHz	766MHz	500MHz	500MHz	566MHz	566MHz		
Intel® Hyper-threading /VT/VTX/Intel® vPro	Yes	Yes	Yes	Yes	Yes	Yes	Yes		
Package	BGA /PGA	BGA /PGA	BGA /PGA	BGA	BGA	BGA	BGA		



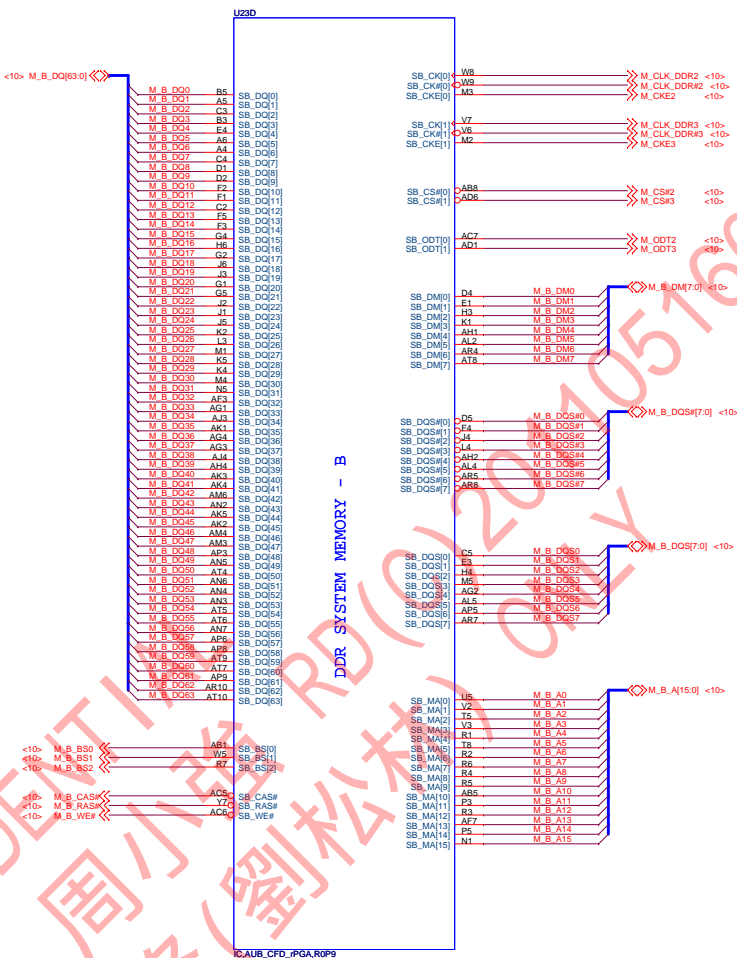
### Coordination of Thread Power States at the Core Level

Processor Core C-State		Thread 1			
		C0	C1	C3	C6
Thread 0	C0	C0	C0	C0	C0
	C1	C0	C1 <sup>1</sup>	C1 <sup>1</sup>	C1 <sup>1</sup>
	C3	C0	C1 <sup>1</sup>	C3	C3
	C6	C0	C1 <sup>1</sup>	C3	C6

ARRANDALE PROCESSOR (DDR3)



**N12-9890030-L06**



**N12-9890030-L06**

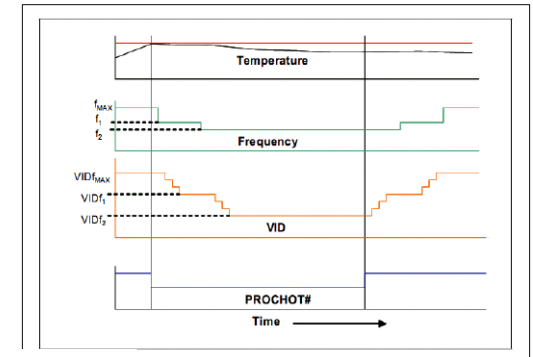
2010/01/12 remove external CLK from CLK GEN

#### Arrandale Reference Clocks

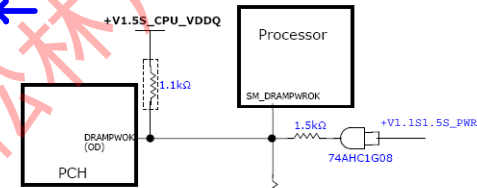
Reference Input Clocks	Input Frequency	Associated PLL
BCLK/BCLK#	133 MHz	Processor/Memory/Graphics
PEG_CLK/PEG_CLK#	100 MHz	PCI Express/DMI/Intel® FDI
DPLL_REF_SSCLK/DPLL_REF_SSCLK#	120 MHz	Embedded DisplayPort (eDP)

Signal Name	Description	Direction/Buffer Type
VCCPWRGOOD_0 VCCPWRGOOD_1	<b>VCCPWRGOOD_0 and VCCPWRGOOD_1 (Power Good) Processor Input:</b> The processor requires these signals to be a clean indication that: -VCC, VCCPLL, and VTT supplies are stable and within their specifications -BCLK is stable and has been running for a minimum number of cycles. Both signals must then transition monotonically to a high state. VCCPWRGOOD_0 and VCCPWRGOOD_1 can be driven inactive at any time, but BCLK and power must again be stable before a subsequent rising edge of these signals. VCCPWRGOOD_0 and VCCPWRGOOD_1 should be tied together and connected to the PROCPWRGD output signal of the PCH.	I Asynchronous CMOS

#### Frequency and Voltage Ordering



#### N12-9890030-L06



SM\_DRAMPWROK signal is driven low when PROCESSOR is turned off in S3 entry. During S3 exit, this signal is driven high only after +V1.5S\_CPU\_VDDQ stable. There is no timing requirement between and 0.75-V  $V_{TT}$  rail.

+V1.1S1.5S\_PWRGD signal is an open-drain signal driven from +V1.5S\_CPU\_VDDQ PWRGOOD logic. It should go high only after +V1.5S\_CPU\_VDDQ to processor is stable.

#### DRAMPWROK behavior in S5/S4 to S0:

During S5/S4 to S0, DRAMPWROK is driven low by PCH until PCH\_PWROK becomes high provided SLP\_S4# is high. Even though DRAMPWROK derived from PWRGOOD of +V1.5S\_CPU\_VDDQ comparator, it is overdriven to low by PCH until PCH\_PWROK goes high. This implementation ensures that S5 to S0 timings are maintained.

#### DRAMPWROK behavior in S0 to S3:

This signal is driven low as the +V1.1S1.5S\_PWRGD becomes low when +V1.5S\_CPU\_VDDQ ramps down. To maintain this signal low, this AND gate is powered using SUS rail (+V3.3A). Any buffer/AND gate of 4 mA should work fine in the given circuit.

#### DRAMPWROK behavior in S3 to S0:

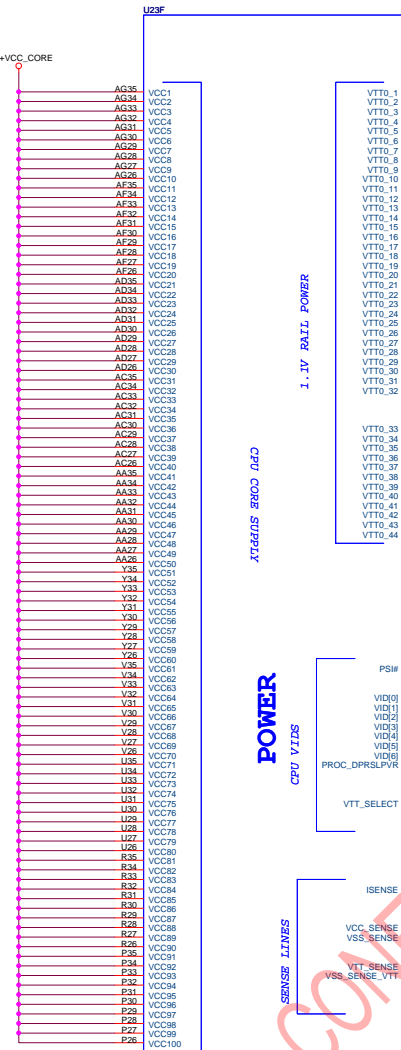
This signal is driven high when +V1.5S\_CPU\_VDDQ to the processor is stable

DRAMPWROK is 1.1-V/1.05-V signal to processor; hence a resistor divider is implemented to level translate the signal.

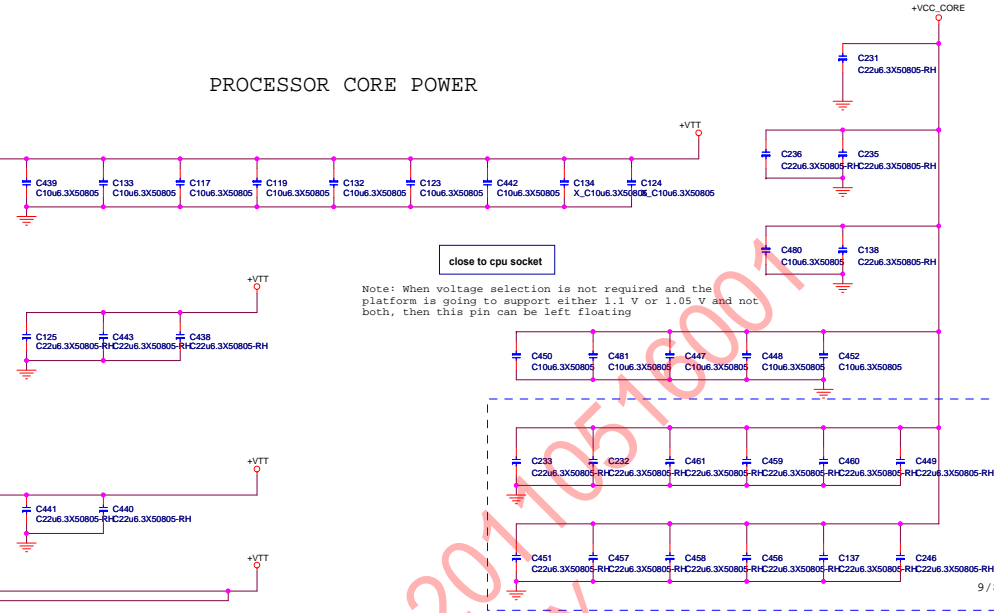
Refer to the latest Intel CRB schematics for more details on +V1.1S1.5S\_PWRGD generation.

ARRANDALE:  
SV=48A  
LV=35A  
ULV=27A

## +VCC\_CORE



## PROCESSOR CORE POWER



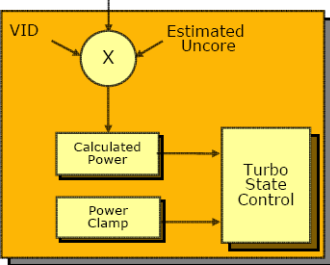
9/

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>TT</sub>	Voltage for the memory controller and shared cache defined at the motherboard V <sub>TT</sub> pinfield via	0.9975	1.05	1.1025	V
	Voltage for the memory controller and shared cache defined across V <sub>TT_SENSE</sub> and V <sub>SS_SENSE_VTT</sub>	0.9765	1.05	1.1235	V
V <sub>DDQ</sub> (DC+AC)	Processor I/O supply voltage for DDR3 (DC + AC specification)	1.425	1.5	1.575	V
V <sub>CCPLL</sub>	PLL supply voltage (DC + AC specification)	1.710	1.8	1.890	V
I <sub>CCMAX_VTT</sub>	Max Current for V <sub>TT</sub> Rail SV LV ULV		-	18 16 16	A
I <sub>CCMAX_VDDQ</sub>	Max Current for V <sub>DDQ</sub> Rail		-	3	A
I <sub>CCMAX_VDDQ_OK</sub>	BGA Only.			0.2	A
I <sub>CCMAX_VTTO_DOR</sub>	BGA Only			2.6	A
I <sub>CCMAX_VCCPLL</sub>	Max Current for V <sub>CCPLL</sub> Rail		-	1.35	A
I <sub>CCTDC_VTT</sub>	Thermal Design Current (TDC) for V <sub>TT</sub> Rail SV LV ULV		-	18 16 16	A
I <sub>CCAVG_VDDQ</sub> (Standby)	Average Current for V <sub>DDQ</sub> Rail during Standby		-	0.33	A

Symbol	Parameter	Segment	Min	Typ	Max	Unit
$I_{CCMAX}$	Maximum Processor Core $I_{CC}$	SV LV ULV			48 35 27	A
$I_{CC\_TDC}$	Thermal Design $I_{CC}$	SV LV ULV			32 22 16	A
$I_{CC\_LPM}$	$I_{CC}$ at LFM	SV LV ULV			18 12 9	A
$I_{CS}$	$I_{CC}$ at C6 Idle-state	SV LV ULV			0.3 0.3 0.3	A



IMON

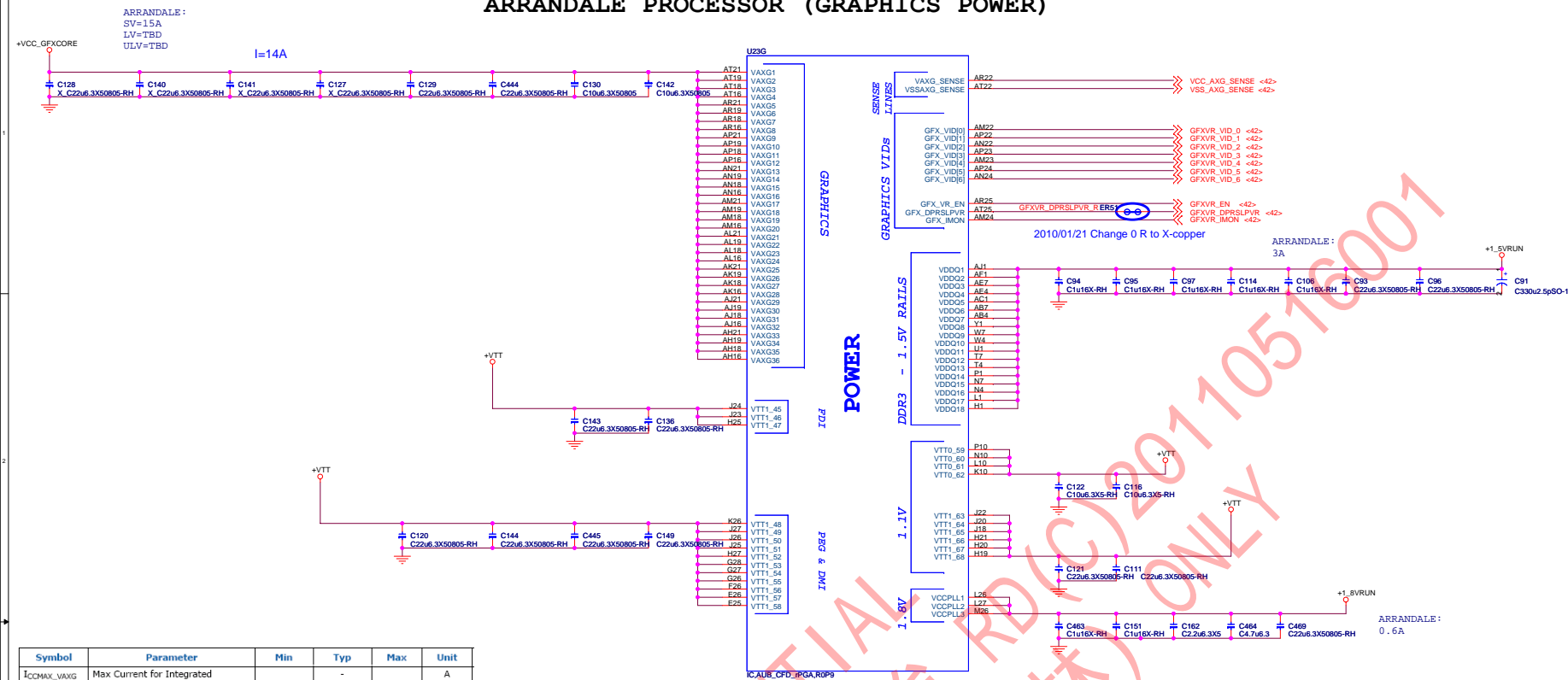
Table 17. IA Core I<sub>MAX</sub> and Gain Definition – Defined Relative to CPU Core Maximum Current

CPU SKU, I <sub>CC</sub> CORE-MAX Maximum CPU Core Current	I <sub>MAX</sub> (IMON) 100 mV [A]	CPU Gain Setting Set on Platform Via CSC Lines	Equivalent Gain [mΩ]
Feature disabled		000	
I <sub>CC</sub> CORE-MAX ≤ 20 A	20	001	45.0
20A < I <sub>CC</sub> CORE-MAX ≤ 30 A	30	010	30.0
30A < I <sub>CC</sub> CORE-MAX ≤ 40 A	40	011	22.5
40A < I <sub>CC</sub> CORE-MAX ≤ 50 A	50	100	18.0
50A < I <sub>CC</sub> CORE-MAX ≤ 60 A	60	101	15.0
60A < I <sub>CC</sub> CORE-MAX ≤ 70 A	70	110	12.9
70A < I <sub>CC</sub> CORE-MAX ≤ 90 A	90	111	10.0

MSID[2]	MSID[1]	MSID[0]	Description <sup>1,2</sup>
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Arrandale Standard Voltage (SV) 35W Supported
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



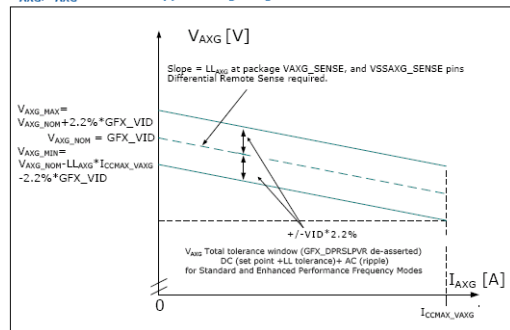
## ARRANDALE PROCESSOR (GRAPHICS POWER)



Symbol	Parameter	Min	Typ	Max	Unit
I <sub>CCMAX_VAXG</sub>	Max Current for Integrated Graphics Rail SV LV ULV		-	22 15 12	A
I <sub>CTDC_VAXG</sub>	Thermal Design Current (TDC) for Integrated Graphics Rail SV LV ULV		-	12 7 6	A

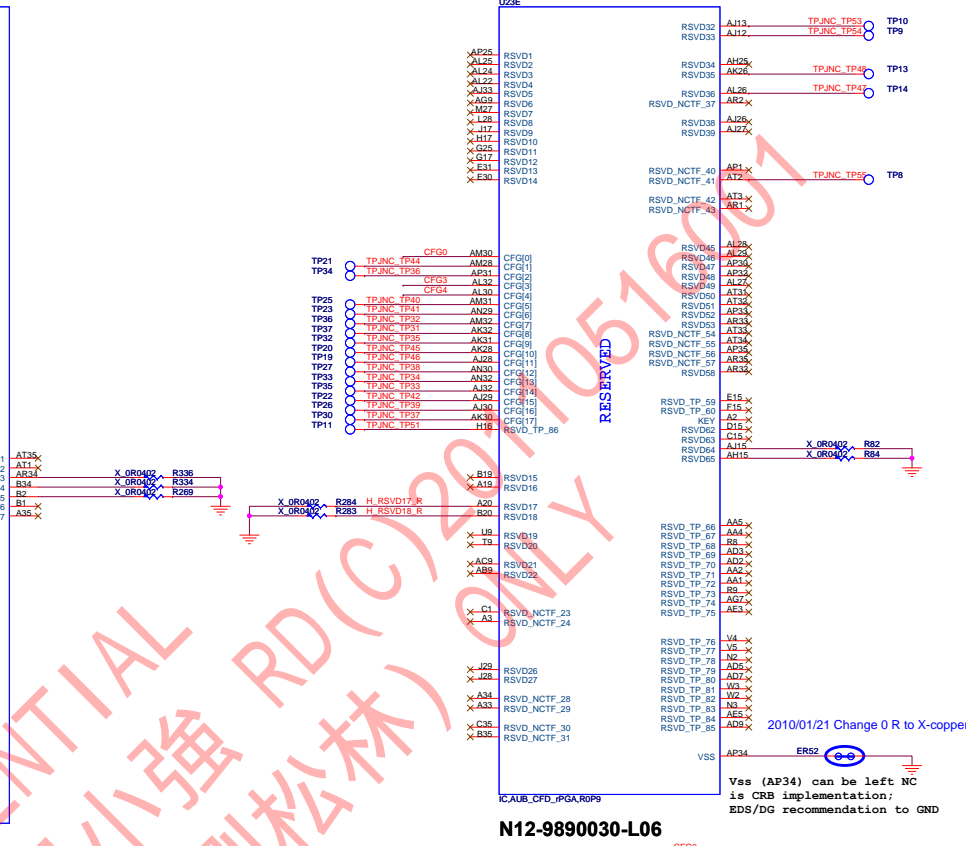
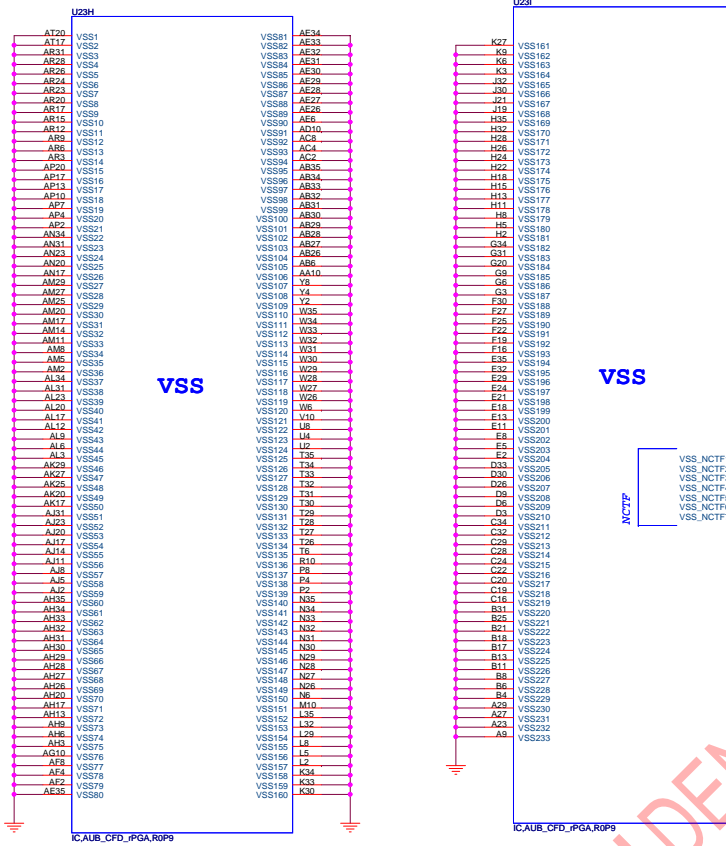
Symbol	Parameter	Min	Typ	Max	Unit
V <sub>AXG</sub>	Graphics core voltage	See Figure 15			

### $V_{AXG}/I_{AXG}$ Static and Ripple Voltage Regulation



## ARRANDALE PROCESSOR (GND)

## ARRANDALE PROCESSOR (RESERVED)



## N12-9890030-L06

## Processor Core/Package State Support

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT state.
C1E	AutoHALT state with lowest frequency and voltage operating point.
C3	Execution cores in C3 flush their L1 instruction cache, L1 data cache, and L2 cache to the L3 shared cache. Clocks are shut off to each core.
C6	Execution cores in this state save their architectural state before removing core voltage.

## Integrated Memory Controller States

State	Description
Power up	CKE asserted, Active mode.
Pre-charge Power down	CKE deasserted (not self-refresh) with all banks closed.
Active Power down	CKE deasserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE deasserted using device self-refresh.

## PCIe Link States

State	Description
L0	Full on - Active transfer state.
L0s	First Active Power Management low power state - Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) - Longest exit latency.

## N12-9890030-L06

## DMI States

State	Description
L0	Full on - Active transfer state.
L0s	First Active Power Management low power state - Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) - Longest exit latency.

## Integrated Graphics Controller States

State	Description
D0	Full on, display active.
D3 Cold	Power-off.

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

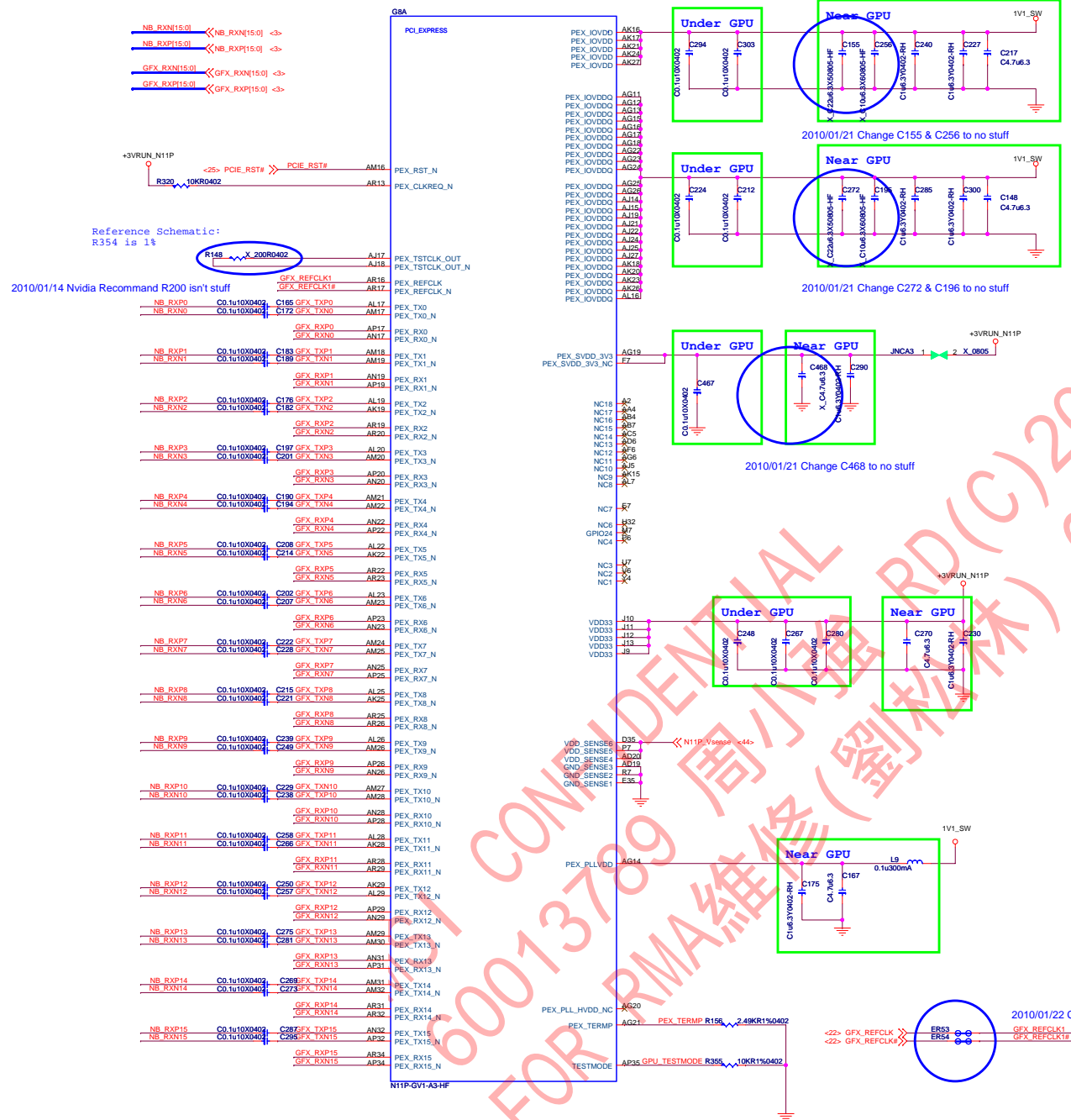
CFG4 - Display Port Presence	
CFG4	1:Disabled: No Physical Display Port attached to Embedded Display Port 0:Enabled: An external Display Port device is connected to the Embedded Display Port

Layout Note:  
Location of all CPU strap resistors needs to be close to trace to minimize stub









**Optimus Software Design for Arrandale Platforms**  
**At POST, the system BIOS should initialize the IGP as the primary graphics adapter. As the OS initializes, both the IGP driver and GPU driver will load. Up to this point the platform is similar to any multiple graphics adapter system-such as a desktop system with more than one graphics card installed. However, the GPU in an Optimus system typically has no physical display outputs. It is purely a graphics rendering and compute device. Then Optimus software will determine when the GPU's capabilities are needed and will enable the GPU as needed, and will host work for individual applications on the GPU as needed.**

DIFFPAIR	IMPEDANCE	CRITICAL
PEX_TX	90DIFF	1
PEX_TX	90DIFF	1
DIFFPAIR	IMPEDANCE	CRITICAL
PEX_RX	90DIFF	1
PEX_RX	90DIFF	1
DIFFPAIR	IMPEDANCE	CRITICAL
PEX_CLK_OUT	90DIFF	1
PEX_CLK_OUT	90DIFF	1

#### SOURCE POWER NETS

NET	MIN_LINE_WIDTH	MAX_CURRENT	VOLTAGE	POWER_NET
3V3	16.00	4A	3.30000V	TRUE
12V	25.00	8A	18.0000V	TRUE

Features	N11P-GE1	N11P-LP1	N11P-GS1
Host Platform	PCI-E 2.0 x 16		
Memory Interface	128-bit DDR3 GDDR3		128-bit DDR3 GDDR3 GDDR5
Process Technology	40nm		
Device ID	0x0A29	0x0A2B	0x0CAF
Package	969-ball BGA 29nm x 29nm package BG1-128		
Display	DVII DVID 1920 x 1200 @ 60Hz	DVII DVID 2560 x 1600 @ 60Hz	



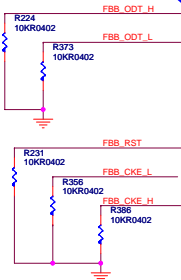
<16,17> FBC\_D[63:0]

<16,17> FBC\_DQM[7:0]

<16,17> FBC\_DQS[7:0]

<16,17> FBC\_DQS[7:0]

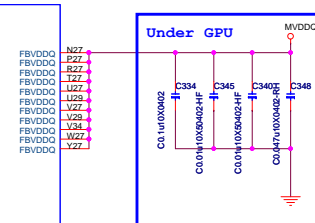
2010/01/14 Change resistor form 1% to 5%



GBC

FBC

FBC\_D0, FBC\_D1, FBC\_D2, FBC\_D3, FBC\_D4, FBC\_D5, FBC\_D6, FBC\_D7, FBC\_D8, FBC\_D9, FBC\_D10, FBC\_D11, FBC\_D12, FBC\_D13, FBC\_D14, FBC\_D15, FBC\_D16, FBC\_D17, FBC\_D18, FBC\_D19, FBC\_D20, FBC\_D21, FBC\_D22, FBC\_D23, FBC\_D24, FBC\_D25, FBC\_D26, FBC\_D27, FBC\_D28, FBC\_D29, FBC\_D30, FBC\_D31, FBC\_D32, FBC\_D33, FBC\_D34, FBC\_D35, FBC\_D36, FBC\_D37, FBC\_D38, FBC\_D39, FBC\_D40, FBC\_D41, FBC\_D42, FBC\_D43, FBC\_D44, FBC\_D45, FBC\_D46, FBC\_D47, FBC\_D48, FBC\_D49, FBC\_D50, FBC\_D51, FBC\_D52, FBC\_D53, FBC\_D54, FBC\_D55, FBC\_D56, FBC\_D57, FBC\_D58, FBC\_D59, FBC\_D60, FBC\_D61, FBC\_D62, FBC\_D63, FBC\_DQM0, FBC\_DQM1, FBC\_DQM2, FBC\_DQM3, FBC\_DQM4, FBC\_DQM5, FBC\_DQM6, FBC\_DQM7, FBC\_DQS\_WP0, FBC\_DQS\_WP1, FBC\_DQS\_WP2, FBC\_DQS\_WP3, FBC\_DQS\_WP4, FBC\_DQS\_WP5, FBC\_DQS\_WP6, FBC\_DQS\_WP7, FBC\_DQS\_RN0, FBC\_DQS\_RN1, FBC\_DQS\_RN2, FBC\_DQS\_RN3, FBC\_DQS\_RN4, FBC\_DQS\_RN5, FBC\_DQS\_RN6, FBC\_DQS\_RN7, FBC\_CLK\_N, FBC\_CLK\_P, FBC\_CLK\_N, FBC\_CLK\_P

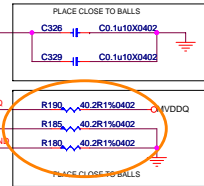


2010/01/21 Change C564 to no stuff

GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FbX_CMD0	FbX_CMD3	CKE	
FbX_CMD1	FbX_CMD8	A8	A8
FbX_CMD2	FbX_CMD21	CAP	
FbX_CMD3	FbX_CMD24	A7	A6
FbX_CMD4	FbX_CMD27	A2	A1
FbX_CMD5	FbX_CMD30	A11	A9
FbX_CMD6	FbX_CMD33	A5	A4
FbX_CMD7	FbX_CMD36	A0	A15
FbX_CMD8	FbX_CMD39	CAS*	CAS*
FbX_CMD9	FbX_CMD42	BA1*	A3
FbX_CMD10	FbX_CMD45	A9*	A11
FbX_CMD11	FbX_CMD48	C0*	
FbX_CMD12	FbX_CMD51	BA0	BA0
FbX_CMD13	FbX_CMD54	BA2	A15
FbX_CMD14	FbX_CMD57	A3	BA1*
FbX_CMD15	FbX_CMD60	C51*	
FbX_CMD16	FbX_CMD63		ODT
FbX_CMD17	FbX_CMD66	A4	A5
FbX_CMD18	FbX_CMD69	A13	A14
FbX_CMD19	FbX_CMD72	WE*	A10
FbX_CMD20	FbX_CMD75	A1	A2
FbX_CMD21	FbX_CMD78	A10	WE*
FbX_CMD22	FbX_CMD81	A0	
FbX_CMD23	FbX_CMD84	C51*	
FbX_CMD24	FbX_CMD87	RA5*	RA5*
FbX_CMD25	FbX_CMD90	ODT	
GB1-128 Mode C Single Bank	GB2-128 Mode E	DRAM Function for DQ Bits 0-31	DRAM Function for DQ Bits 32-63
FbX_CMD26	FbX_CMD93	A6	A7
FbX_CMD27	FbX_CMD96		CKE
FbX_CMD28	FbX_CMD99	RST	RST
FbX_CMD29	FbX_CMD102	A14	A13
FbX_CMD30	FbX_CMD105	A15	BA2
Not Available	FbX_CMD108		

FBB\_ODT\_L <16>  
FBB\_C0\_L <16>  
FBB\_CKE\_L <16>  
FBB\_A9\_A11 <16,17>  
FBB\_A8\_A7 <16,17>  
FBB\_A3\_BA1 <16,17>  
FBB\_A0\_A12 <16,17>  
FBB\_A8 <16,17>  
FBB\_A12\_A0 <16,17>  
FBB\_A1\_A2 <16,17>  
FBB\_A18 <16,17>  
FBB\_A19\_A16 <16,17>  
FBB\_A17\_A6 <16,17>  
FBB\_A4\_A5 <16,17>  
FBB\_A11\_A9 <16,17>  
FBB\_CKE\_H <17>  
FBB\_C0\_H <17>  
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FBB\_RST <17>  
FBB\_A7\_A6 <16,17>  
FBB\_A4\_A5 <16,17>  
FBB\_A2\_A1 <16,17>  
FBB\_A10\_WE <16,17>  
FBB\_A9\_A4 <16,17>  
FBB\_BA2\_A15 <16,17>  
FBB\_VIE\_A10 <16,17>  
FBB\_BA0 <16,17>  
FBB\_A15\_BA2 <16,17>  
FBB\_CLK\_N <16>  
FBB\_CLK\_P <16>  
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FBB\_CLK\_P <17>

2010/01/26 reserve for Nvidia request



NV Check those value is correct

2101/01/25 Resistor PN peding change to R11-402AT12-W08

R11-604AT12-W08

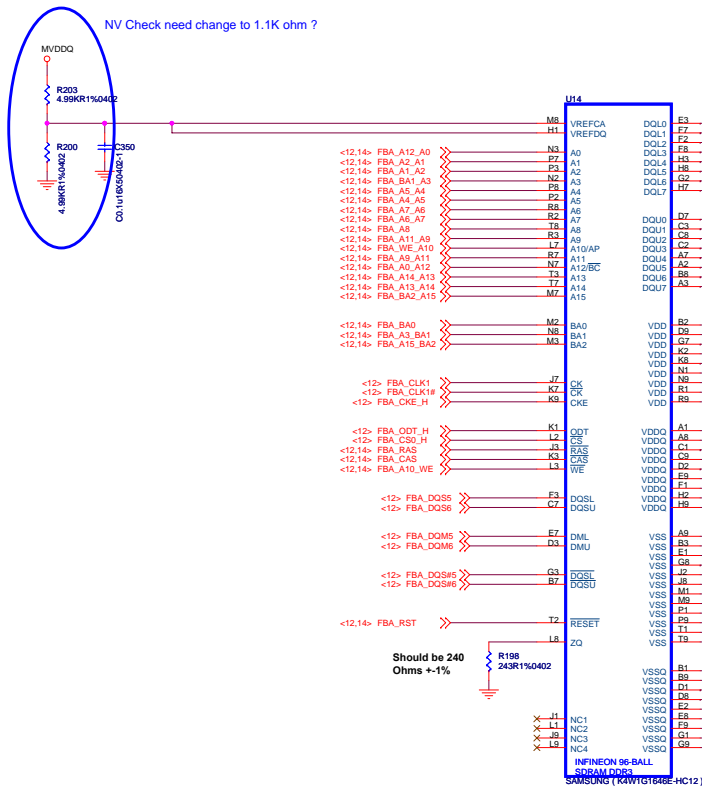
2010/3/14 For Nvidia suggestion change R190 value form 60R to 40R

NET	NV_IMPEDANCE	CRITICAL
FB_CAL_PD_VDDQ	50OHM	2
FB_CAL_PU_GND	50OHM	2
FB_CAL_TERM_GND	50OHM	2

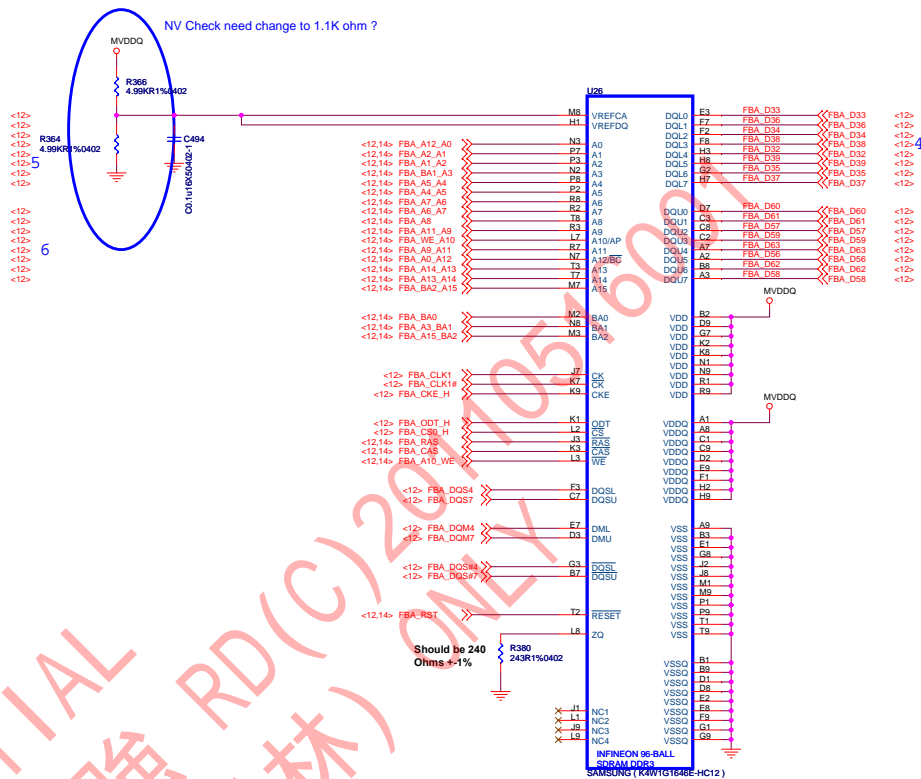




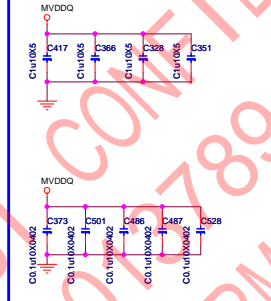
NV Check need change to 1.1K ohm ?



NV Check need change to 1.1K ohm ?

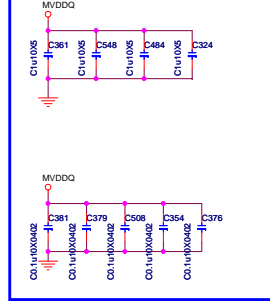


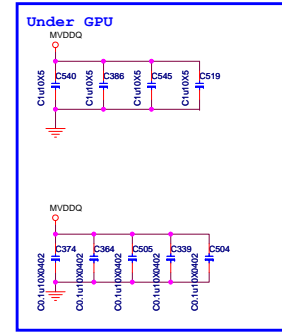
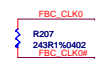
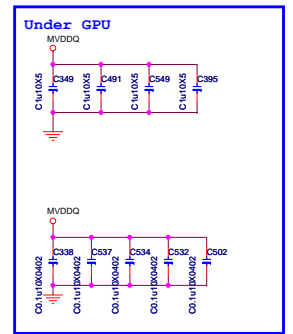
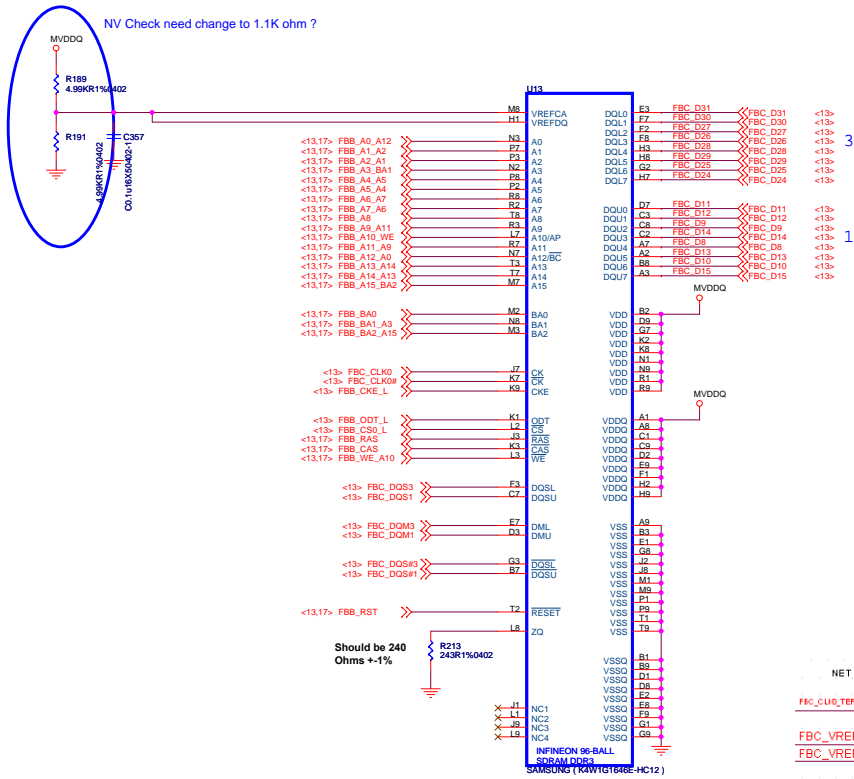
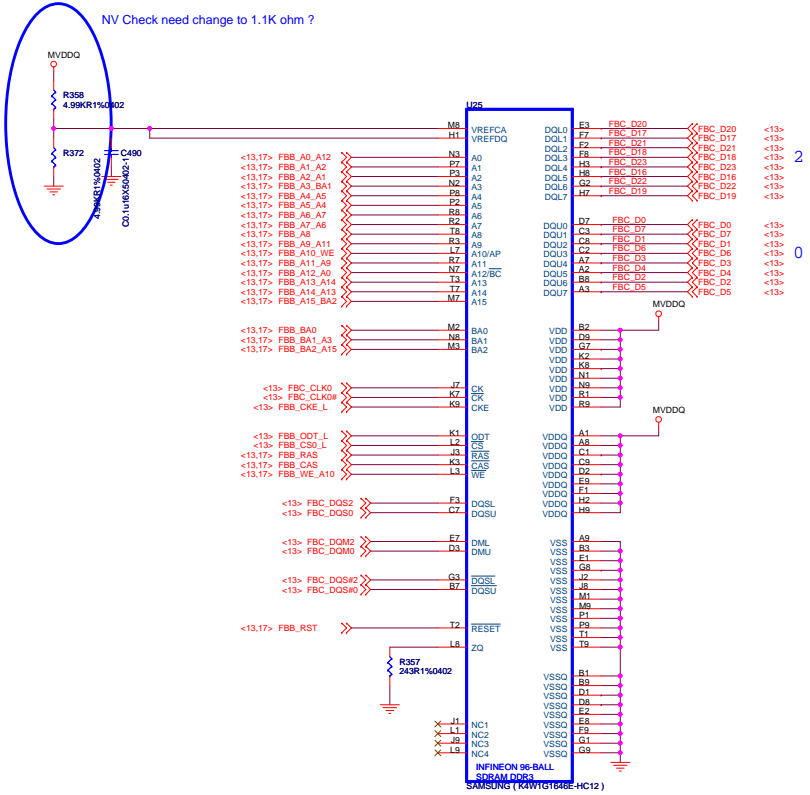
Under GPU



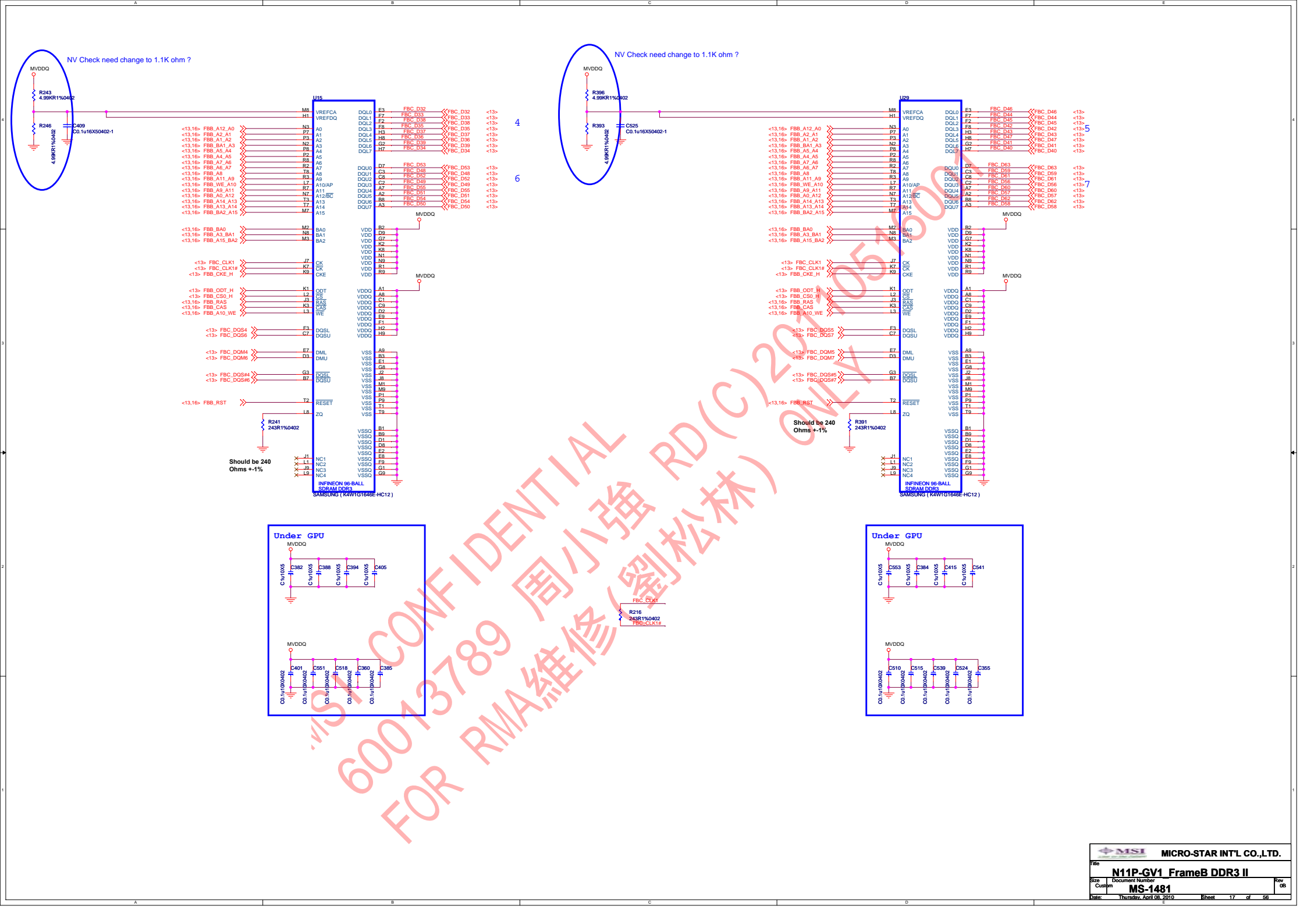
NET	MIN_LINE_WIDTH	VOLTAGE
FBA_CLK0_TERM		1.05V
FBA_VREF_DQ0	16MIL	0.9V
FBA_VREF_CA0	16MIL	0.9V
FBA_ZQ0	12MIL	0.9V
FBA_ZQ1	12MIL	0.9V

Under GPU





NET	MIN_LINE_WIDTH	VOLTAGE
FBC_CLK0_TERRM		1.05V
FBC_VREF_DQ0	16MIL	0.9V
FBC_VREF_CA0	16MIL	0.9V
FBC_Z00	12MIL	0.9V
FBC_Zq1	12MIL	0.9V







2010/03/16 Modify R157,R160 value from 40.2R to 40.2K



2010/01/14 Change value form 1% to 5%



DA-04881-001\_V04

DA-04882-001

Products	GPU (W)	Mem (W)	NVCLK/MCLK (MHz)
N11P-G01 1024MB DDR3	22.96	5.07	575/790
N11P-LP1 1024MB DDR3	14.81	4.78	475/700
N11P-G01 1024MB DDR3	22.85	4.97	450/790

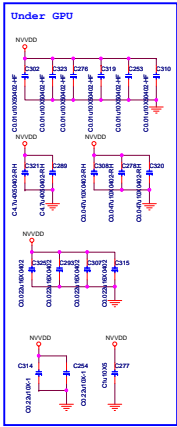
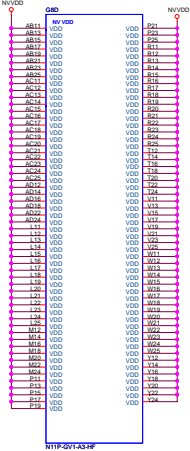
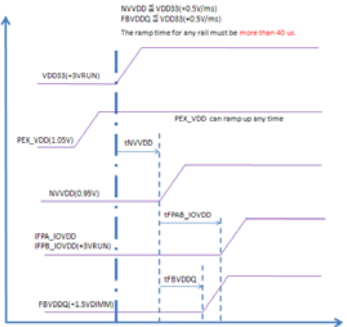
Products	NVYDD
N11P-G01 1024MB DDR3	0.95V 21.4A 20.33W
N11P-LP1 1024MB DDR3	0.85V 14.37A 12.22W
N11P-G01 1024MB DDR3	0.9V 22.19A 19.97W

Products	FBVDD 1.5V		FBVDDQ GPU+Mem 1.5V	
N11P-G01 1024MB DDR3	1.84A	2.76W	2.56A	3.84W
N11P-LP1 1024MB DDR3	1.69A	2.54W	2.48A	3.73W
N11P-G01 1024MB DDR3	1.52A	2.28W	2.98A	4.48W

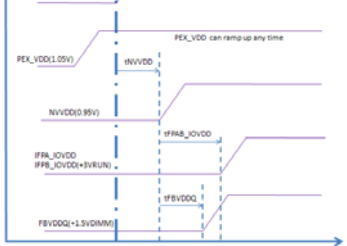
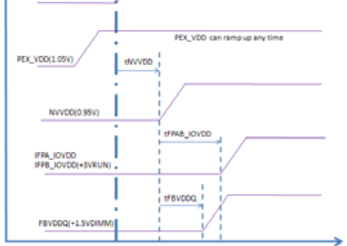
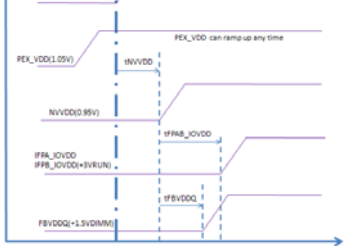
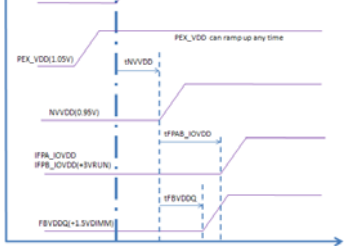
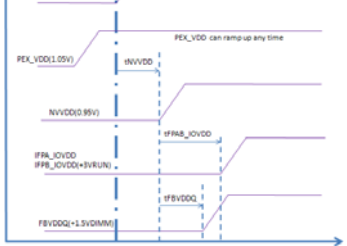
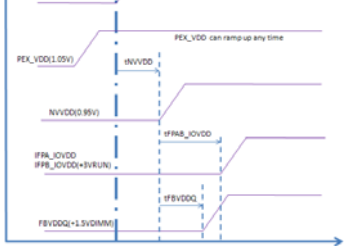
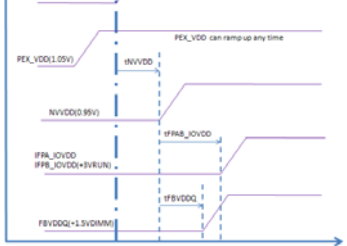
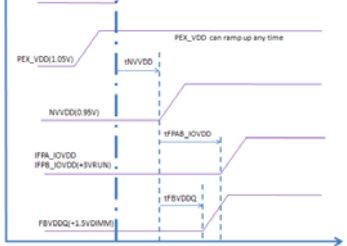
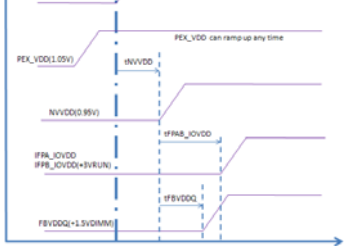
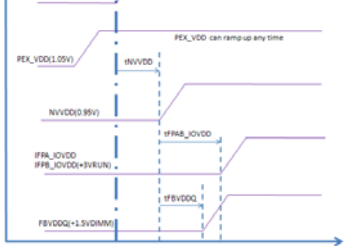
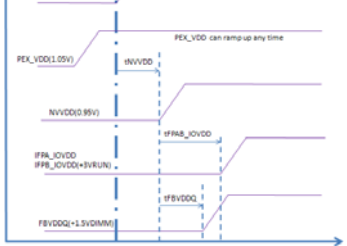
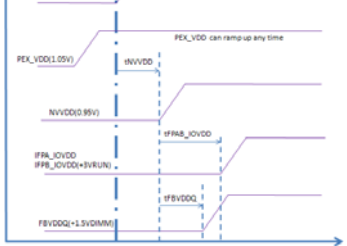
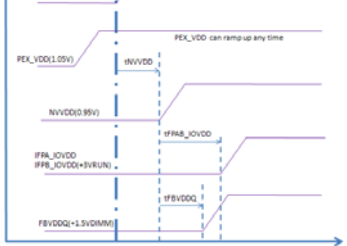
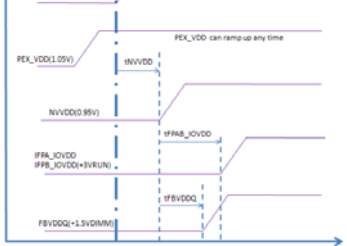
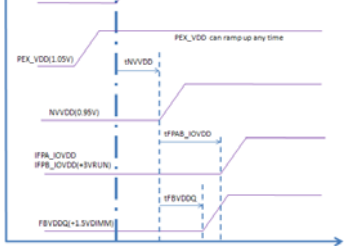
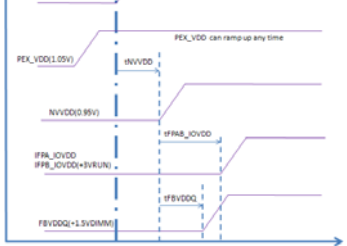
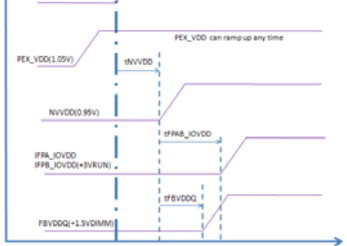
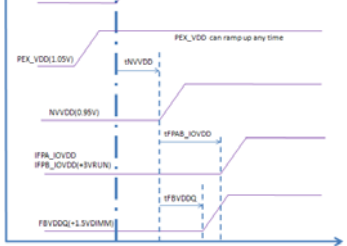
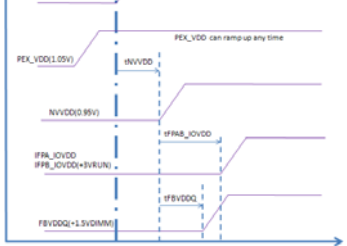
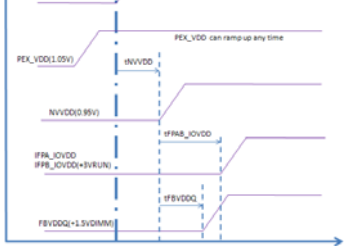
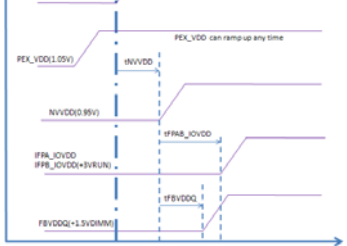
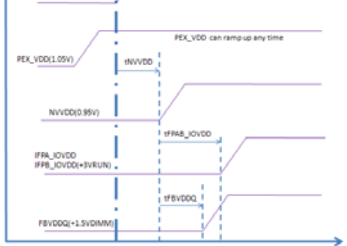
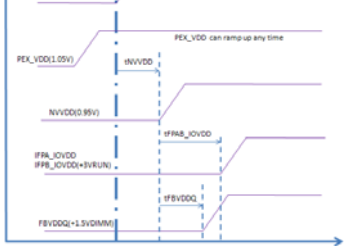
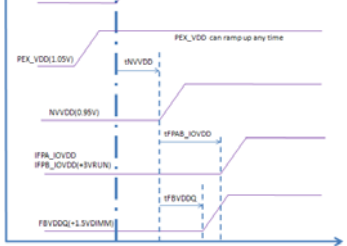
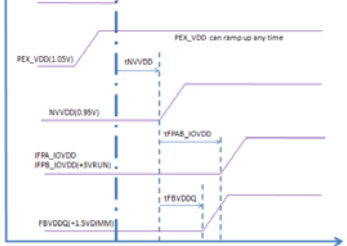
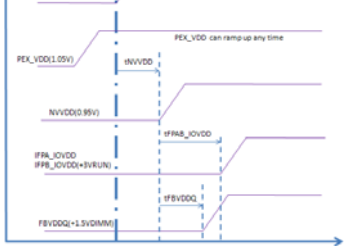
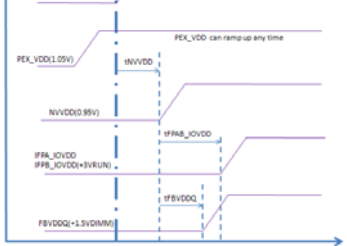
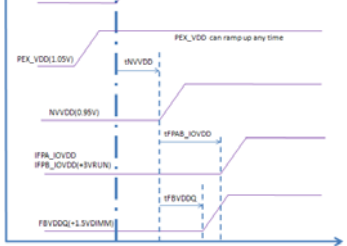
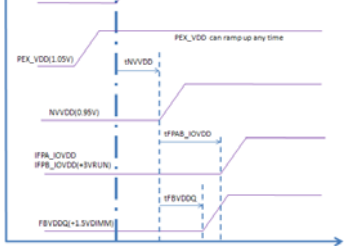
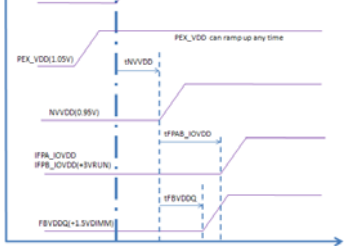
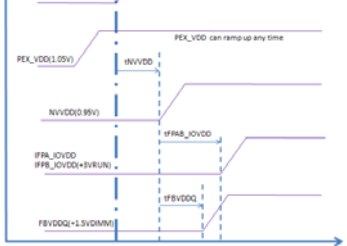
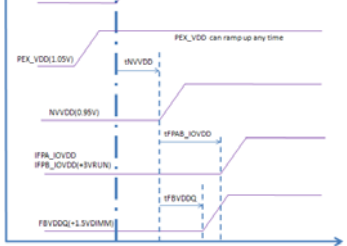
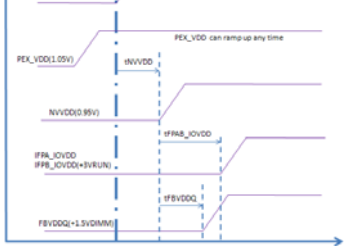
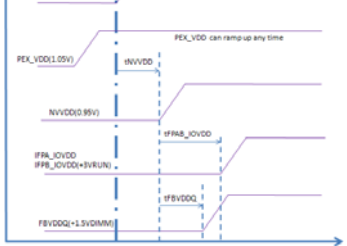
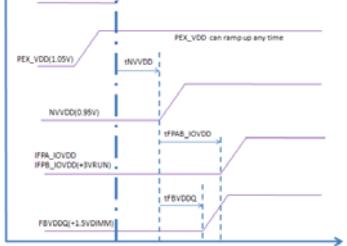
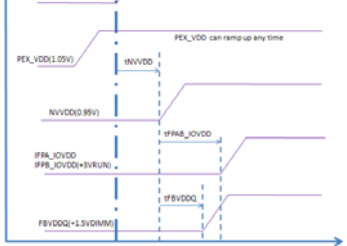
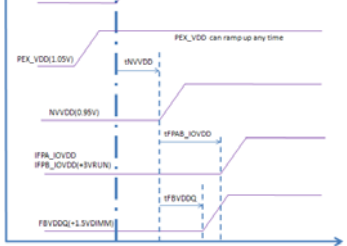
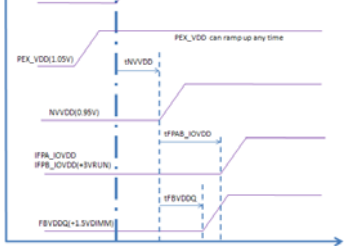
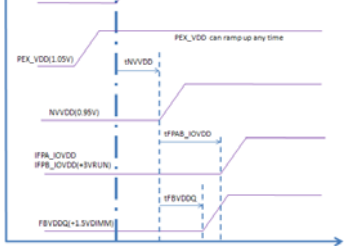
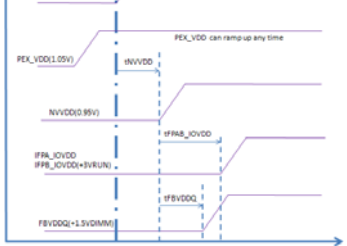
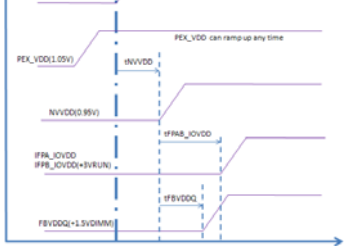
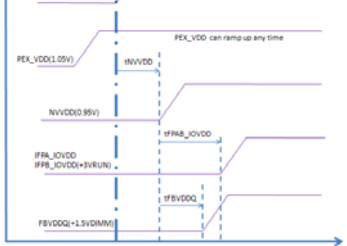
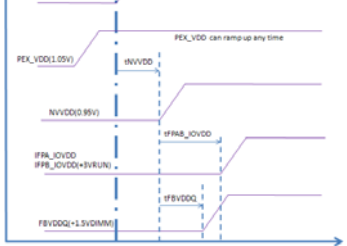
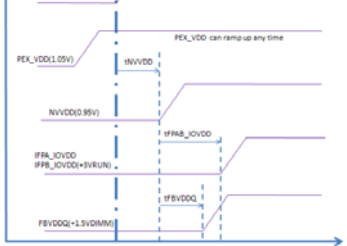
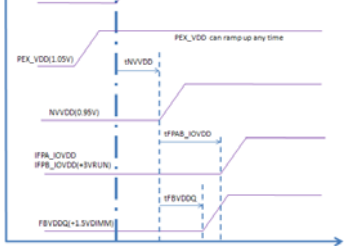
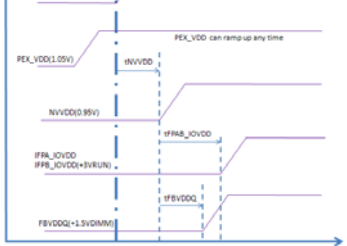
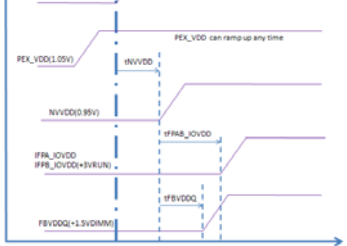
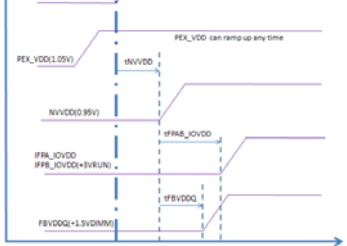
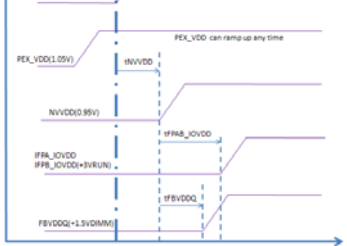
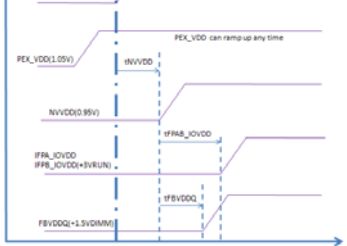
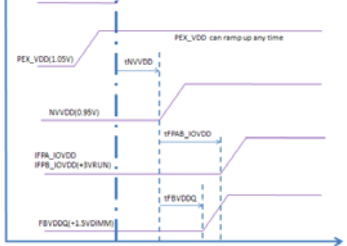
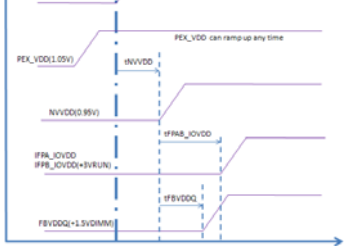
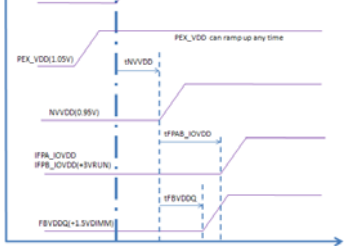
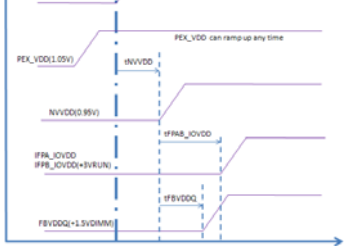
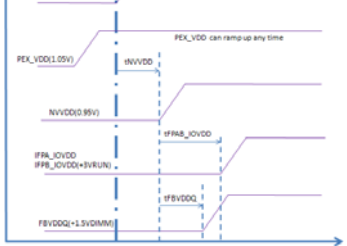
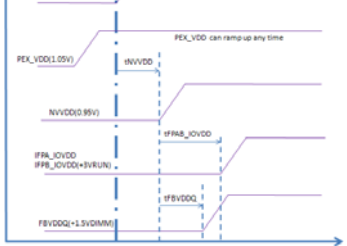
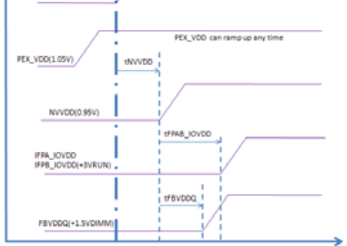
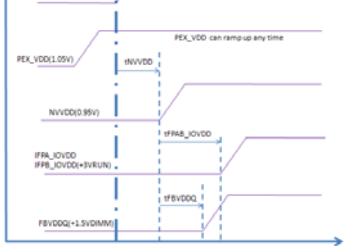
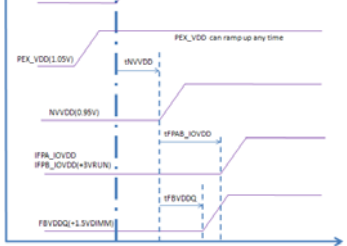
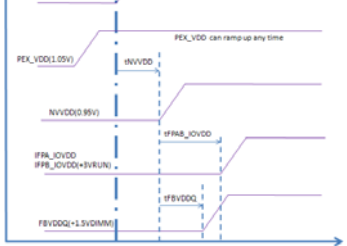
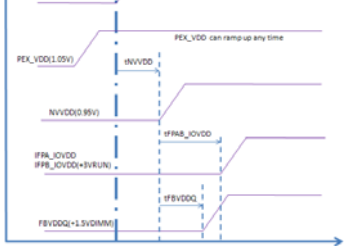
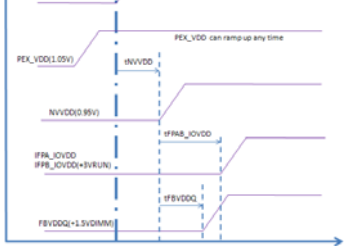
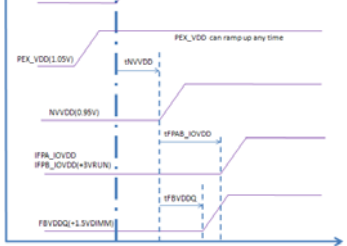
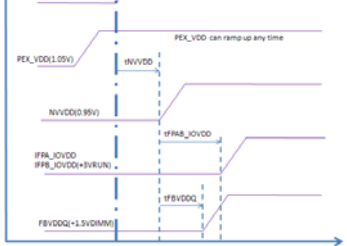
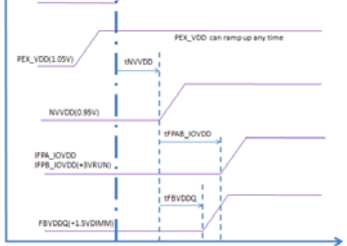
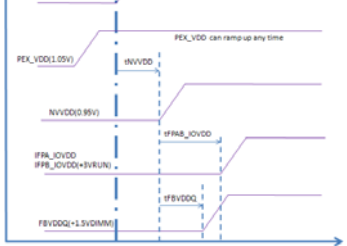
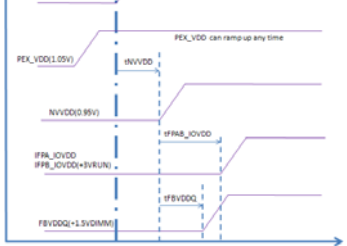
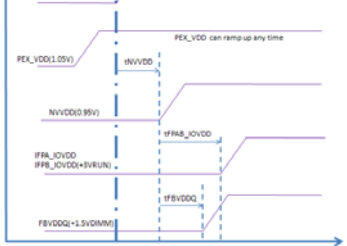
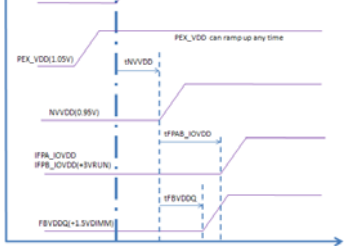
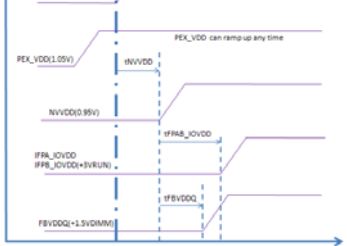
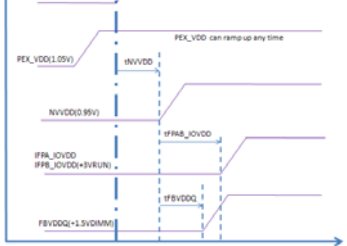
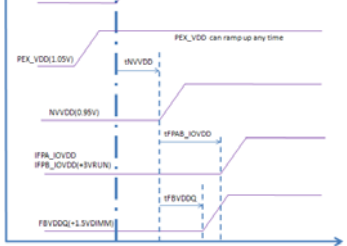
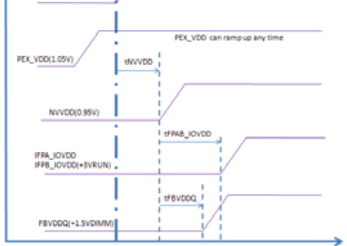
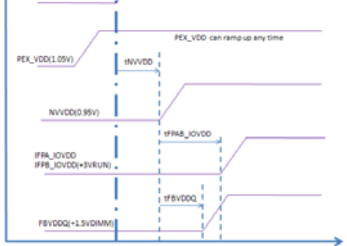
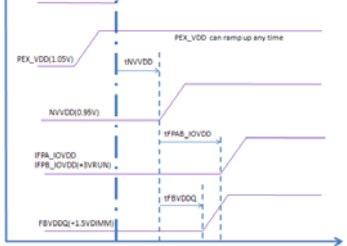
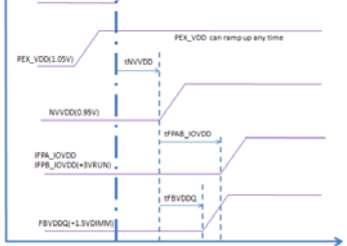
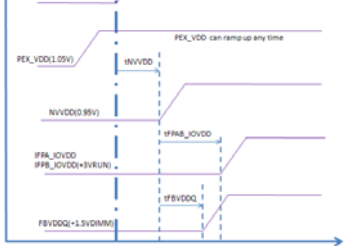
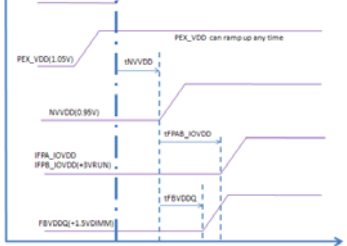
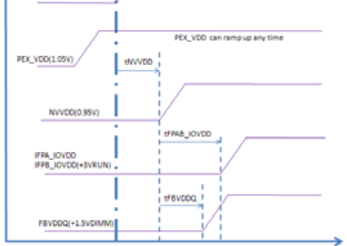
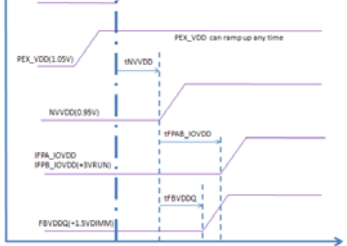
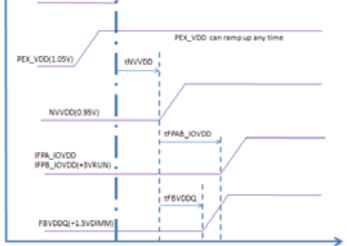
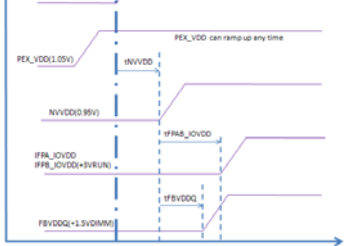
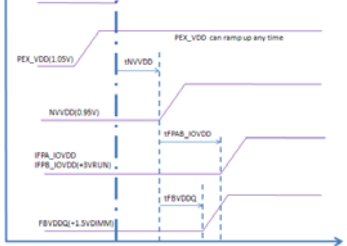
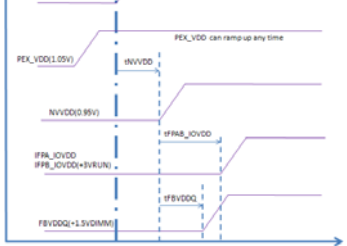
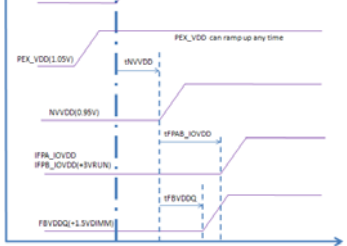
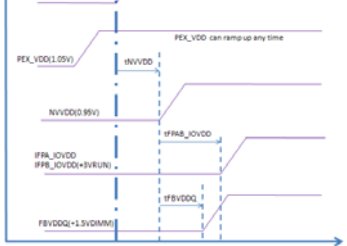
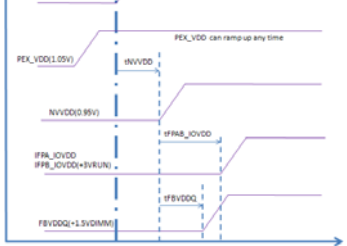
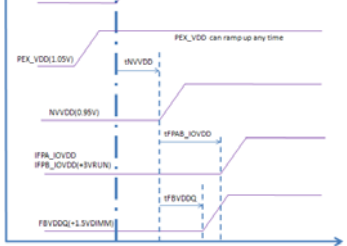
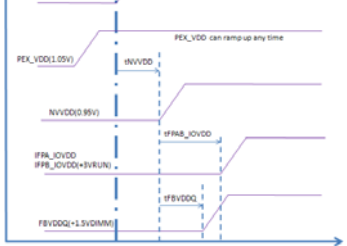
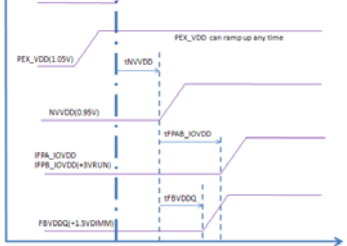
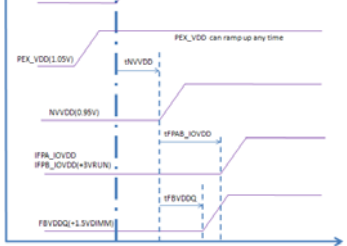
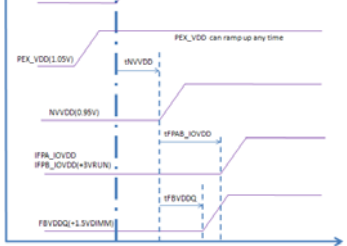
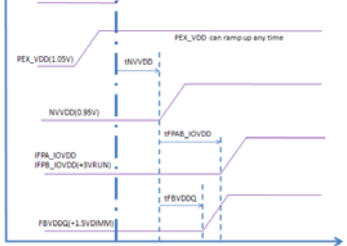
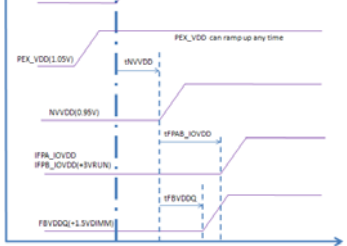
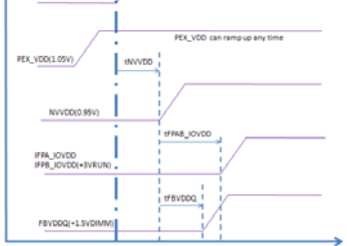
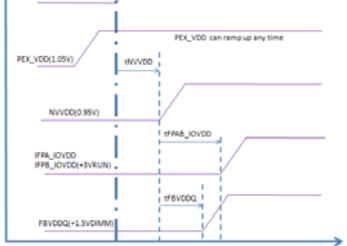
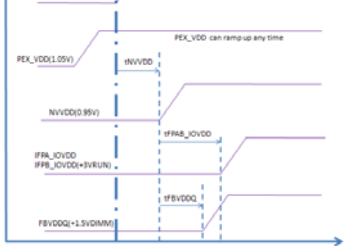
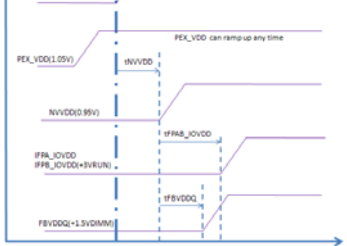
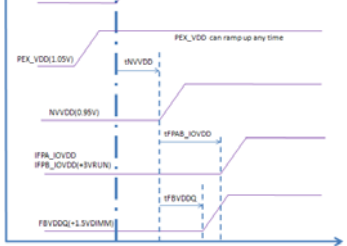
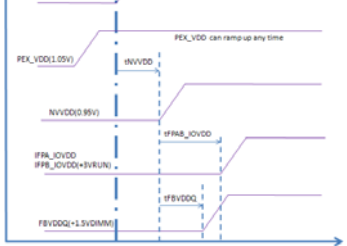
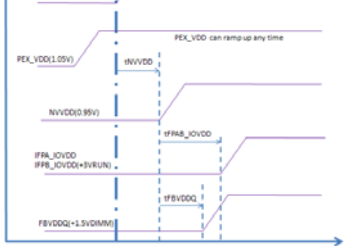
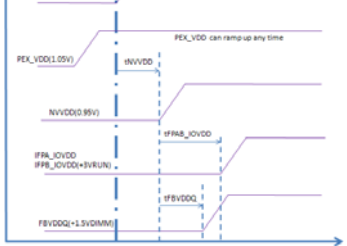
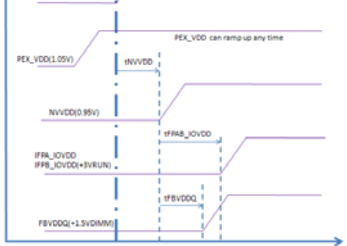
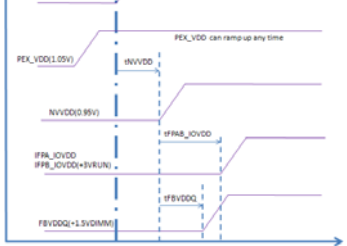
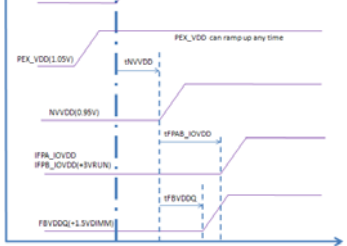
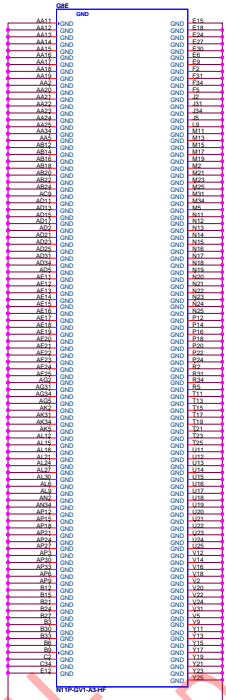
Products	PCI Express 1.05V	IO PLLVDD 1.05V
N11P-G01 1024MB DDR3	599.27mA 0.63W	186.77mA 0.2W
N11P-LP1 1024MB DDR3	581.74mA 0.61W	186.77mA 0.2W
N11P-G01 1024MB DDR3	578mA 0.61W	186mA 0.2W

Products	IO PLLVDD 1.8V
N11P-G01 1024MB DDR3	88.5mA 0.16W
N11P-LP1 1024MB DDR3	88.5mA 0.16W
N11P-G01 1024MB DDR3	87mA 0.16W

Products	Other 3.3V
N11P-G01 1024MB DDR3	39.97mA 0.13W
N11P-LP1 1024MB DDR3	39.97mA 0.13W
N11P-G01 1024MB DDR3	39mA 0.13W

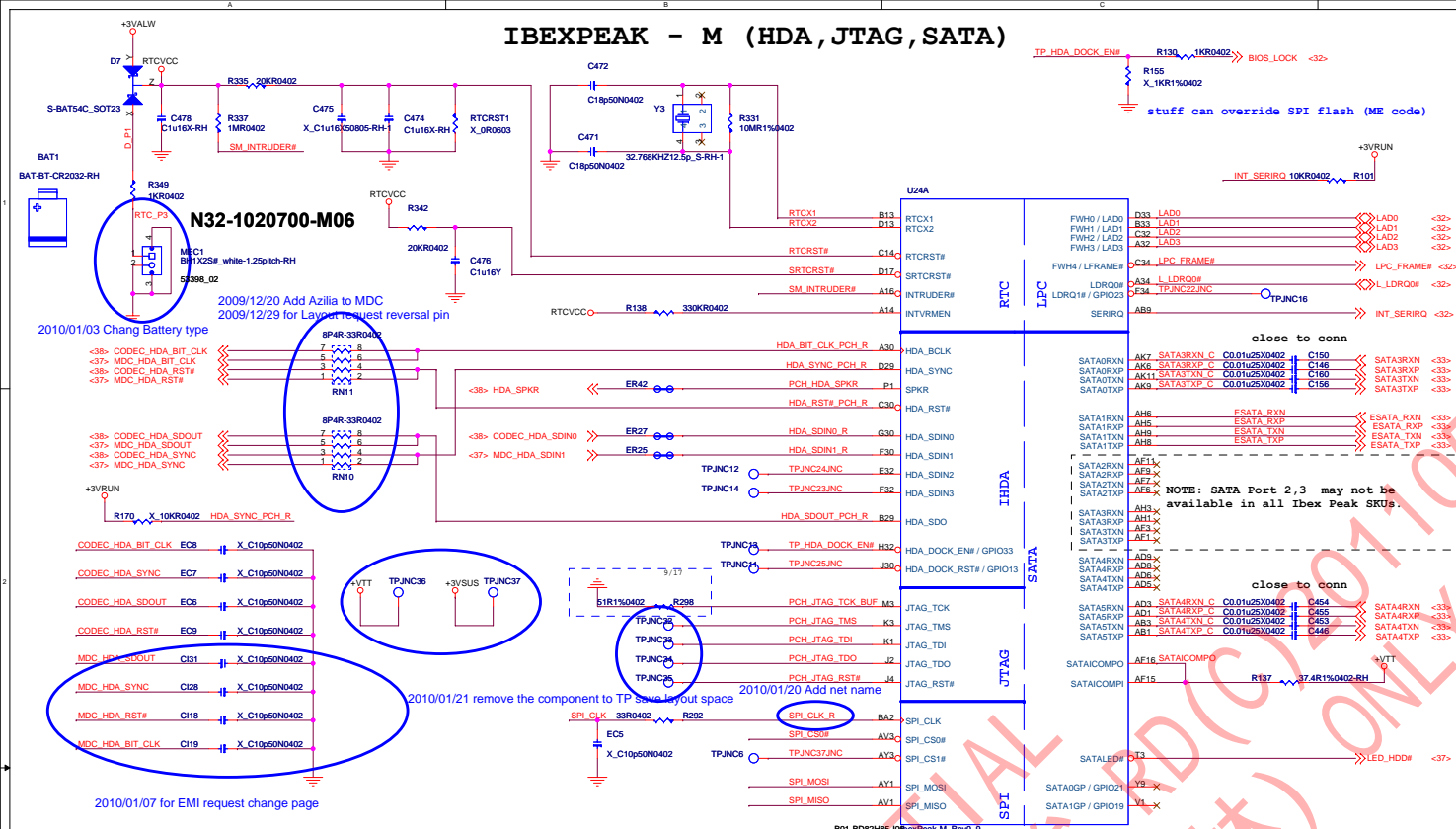


Near GPU





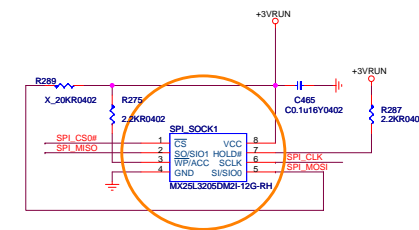
**IBEXPEAK - M (HDA, JTAG, SATA)**



2010/01/21 remove the component to TP save layout space

		Pre-Production Systems		Production Systems
PCH Pin	RefDes	ES1	ES2	
TDO	R1	No Stiff	200 Ohms	No Stiff
	R2	No Stiff	100 Ohms	No Stiff
	R3	200 Ohms	200 Ohms	No Stiff
THS	R4	100 Ohms	100 Ohms	No Stiff
	R5	200 Ohms	200 Ohms	No Stiff
TDI	R6	100 Ohms	100 Ohms	No Stiff
TCK	R7	51 Ohms	51 Ohms	51 Ohms
TRST#	R8	20K Ohms	Not Applicable <sup>1</sup>	Not Applicable <sup>1</sup>
	R9	10K Ohms	Not Applicable <sup>1</sup>	Not Applicable <sup>1</sup>

**Note 1:** For IBX ES2 and later, TRST# does not require an external pull-up; but should be routed to a test point pad for PCH JTAG debug purposes



2010/03/29 remove socket modify to ROM



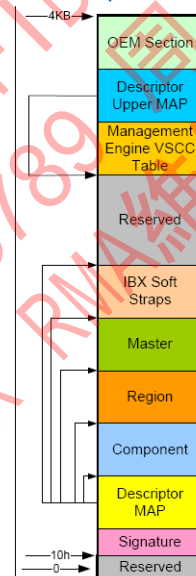
### Boot Flow for Ibex Peak

When booting from Global Reset the PCH SPI controller will look for a descriptor signature on the SPI flash device on Chip Select 0 at address 0x0. The descriptor fetch is triggered whichever comes first, the assertion of `MEPVWROK` or deassertion of `LAN_RST#`. If the signature is present and valid, then the PCH controller will boot in descriptor mode. It will load up the descriptor into corresponding registers in the PCH. If the signature is NOT present the PCH will boot in non descriptor mode where integrated LAN and all Intel Management Firmware will be disabled. Whether there is a valid descriptor or not, the PCH will look to the GNT0# and SPI\_CS1#1 (Boot BIOS Destination straps) to determine if BIOS is to be booted from Firmware hub or SPI flash.

The Flash Descriptor is a data structure that is programmed on the SPI flash part on Ibex Peak based platforms. The Descriptor data structure describes the layout of the flash as well as defining configuration parameters for the PCH. The descriptor is on the SPI flash itself and is not in memory mapped space like PCH programming registers.

The maximum size of the Flash Descriptor is 4 KBytes. It requires its own discrete erase block, so it may need greater than 4 KBytes of flash space depending on the flash architecture that is on the target system.

The information stored in the Flash Descriptor can only be written during the manufacturing process as its read/write permissions must be set to Read Only when the computer leaves the manufacturing floor.

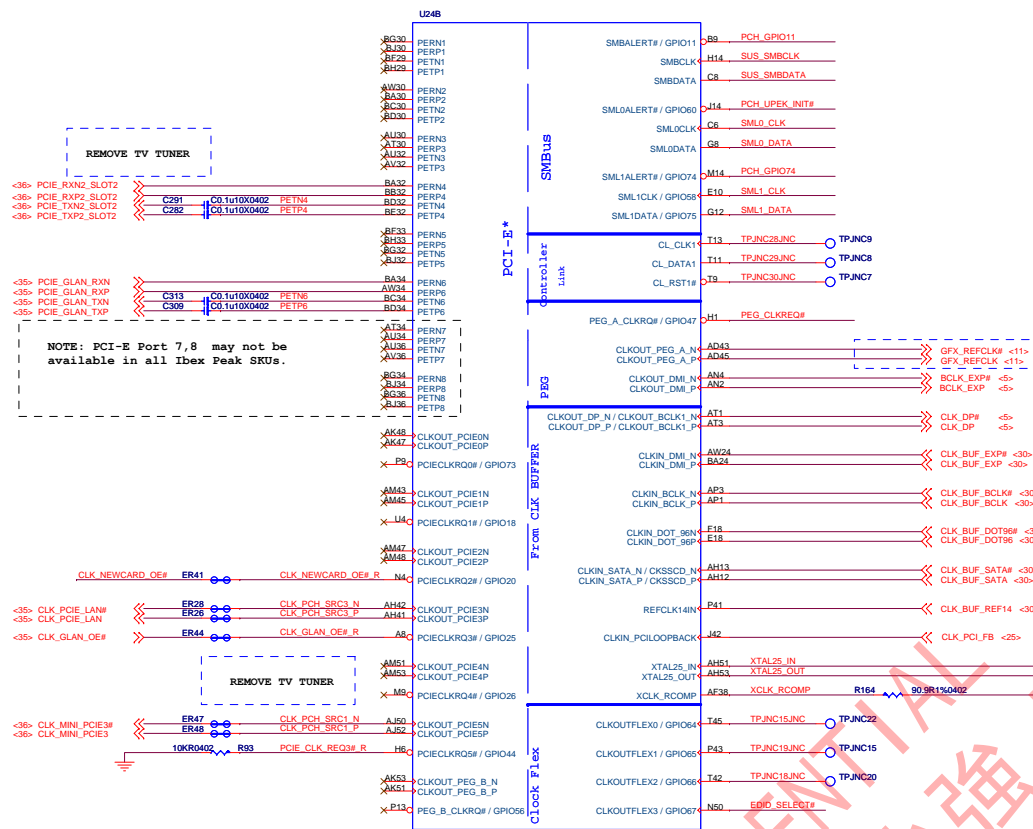


- The Flash signature at the bottom of the flash (offset 0) must be 0FF0A55Ah in order to be in Descriptor mode.
- The Descriptor map has pointers to the lower five descriptor sections as well as the size of each.
- The Component section has information about the SPI flash part(s) the system. It includes the number of components, density of each component, read, write and erase frequencies and invalid instructions.
- The Region section defines the base and the limit of the BIOS, ME and GbE regions as well as their size.
- The master region contains the hardware security settings for the flash, granting read/write permissions for each region and identifying each master.
- PCH chipset soft strap sections contain PCH configurable parameters.
- The Reserved region is for future chipset usage.
- The Descriptor Upper Map determines the length and base address of the Intel® ME VSCC Table.
- The Intel® ME VSCC Table holds the JEDEC ID and the ME VSCC information for all the SPI Flash part(s) supported by the NVM image. This table is **NOT used by Intel® ME Ignition FW** only. BIOS and GbE write and erase capabilities depend on **LVSCC** and **UVSCC** registers in SPIBAR memory space.
- OEM Section is 256 Byte section reserved at the top of the Flash Descriptor for use by the OEM.

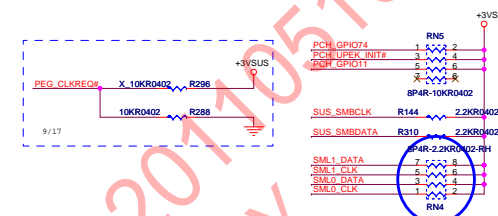
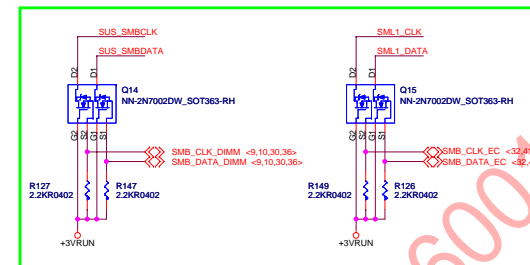
### Region Access Control Table

Master Read/Write Access			
Region	CPU and BIOS	ME	GbE Controller
Descriptor	N/A	N/A	N/A
BIOS	CPU and BIOS can always read from and write to BIOS Region	Read / Write	Read / Write
Management Engine	Read / Write	ME can always read from and write to ME Region	Read / Write
Gigabit Ethernet	Read / Write	Read / Write	GbE software can always read from and write to GbE region
Platform Data Region	N/A	N/A	N/A

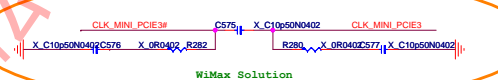
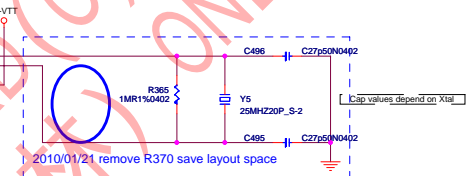
# IBEXPEAK - M (PCI-E, SMBUS, CLK)



PCIECLKRQ1# / GPIO18 PCIECLKRQ1# / GPIO20	RUN Well
PCIECLKRQ0# and PCIECLKRQ3# ~ PCIECLKRQ7# PEG_A_CLKRQ# / PEG_B_CLKRQ#	SUS Well



2009/12/29 RN8 reversal for layout request



2010/03/23 Resever Wimax solution

- EC can read from PCH via SMBus:
  - Temperatures
  - CPU, GMCH
  - Sequence number
  - Host status

- EC can write to PCH via SMBus:
  - Disable and enable power sharing
  - CPU and package power clamps
  - Biasing preference
  - Upper and lower temperature limits
  - CPU, MCH
  - TEMP\_ALERT# trip points

- PCH can alert EC to out of range temperature conditions
- TEMP\_ALERT# signal assertion

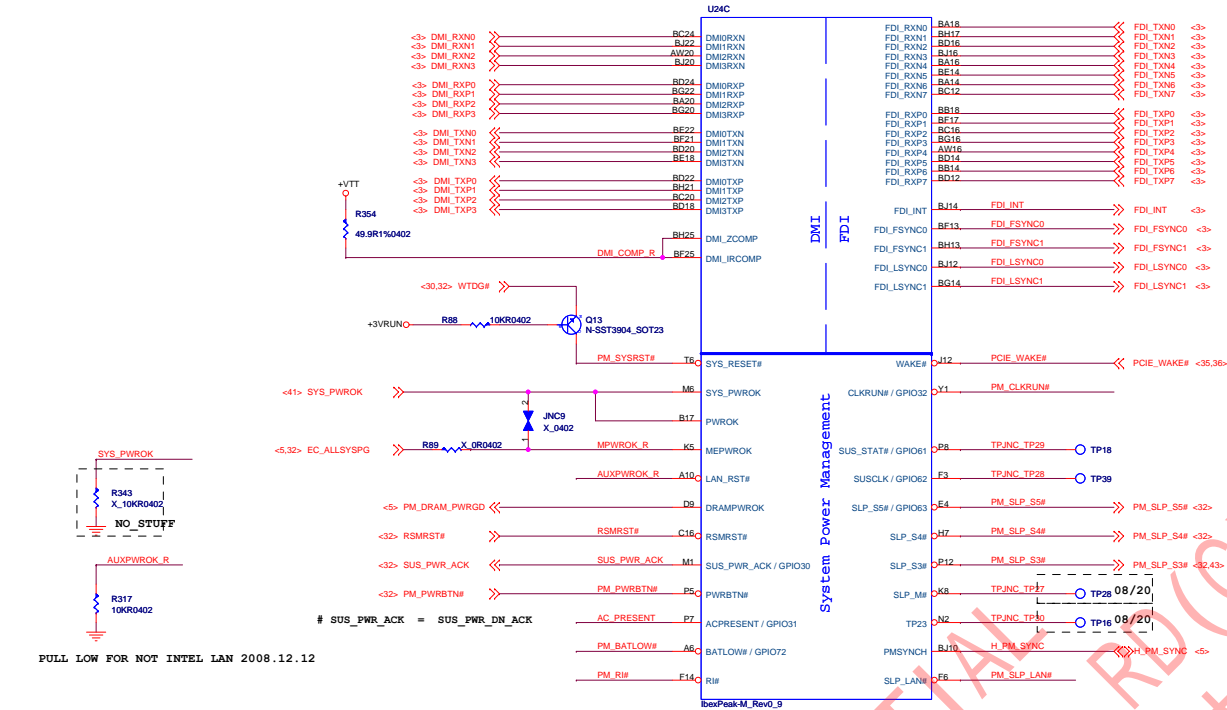
- EC can monitor Intel® ME health by checking "Sequence Number"
- Indicates optional usage with Turbo Boost

- Turbo Boost control- EC passes parameters through PCH to host software for real-time Turbo Boost control.
- PCH can be programmed to notify EC when a device is outside of limits via TEMP\_ALERT# signal- No SW alert in PCH.

Byte	Data	Format	Units	Range
0	Max Package Temperature	Unsigned byte	1°C/bit	0-255°C
1	PCH Temperature	Unsigned byte	1°C/bit	0-255°C
3:2	CPU Temperature	10.6 Format	1/64°C/bit	0-256°C
4	MCH Temperature	Unsigned byte	1°C/bit	0-255°C
5	DIMM0 Temperature	Unsigned byte	1°C/bit	0-255°C
6	DIMM1 Temperature	Unsigned byte	1°C/bit	0-255°C
7	DIMM2 Temperature	Unsigned byte	1°C/bit	0-255°C
8	DIMM3 Temperature	Unsigned byte	1°C/bit	0-255°C
9	Sequence Number	Unsigned byte	Count	0-255
13:10	CPU Energy Counter	16 int:16frac	0.125J/bit	
19:14	Host Status	Status register	N/A	N/A

Commands	Format	Units
SMBus Turbo Status (STS)	Register	
CPU Temperature Limits	10.6 Format	1/64°C/bit
MCH Temperature Limits	Unsigned byte	1°C/bit
IBX Temperature Limits	Unsigned byte	1°C/bit
DIMM Temperature Limits	Unsigned byte	1°C/bit
Processor Power Clamp	Unsigned word	0.1W/bit

# IBEXPEAK - M (DMI, FDI, GPIO)



## Flexible Display Interface

The Flexible Display Interface (Intel® FDI) is a bus technology that utilizes differential signaling to transport display data from a pixel source Havendale to a sink Ibex Peak. There are two Flexible Display Interface channels- A and B which are independently controlled. Each channel from Havendale include 4 Tx differential pairs comprising the data link, used for transporting pixel and framing data from the display engine. Two single-ended LineSync and FrameSync inputs. Single-ended DISP\_INT is used for interrupts from sink (Ibex Peak) to source (Havendale).

Source	Dest	Signal Name
Board	PCH	PWROK
PCH	Processor	DRAMPWRGD
PCH	Processor	PROCWRGD

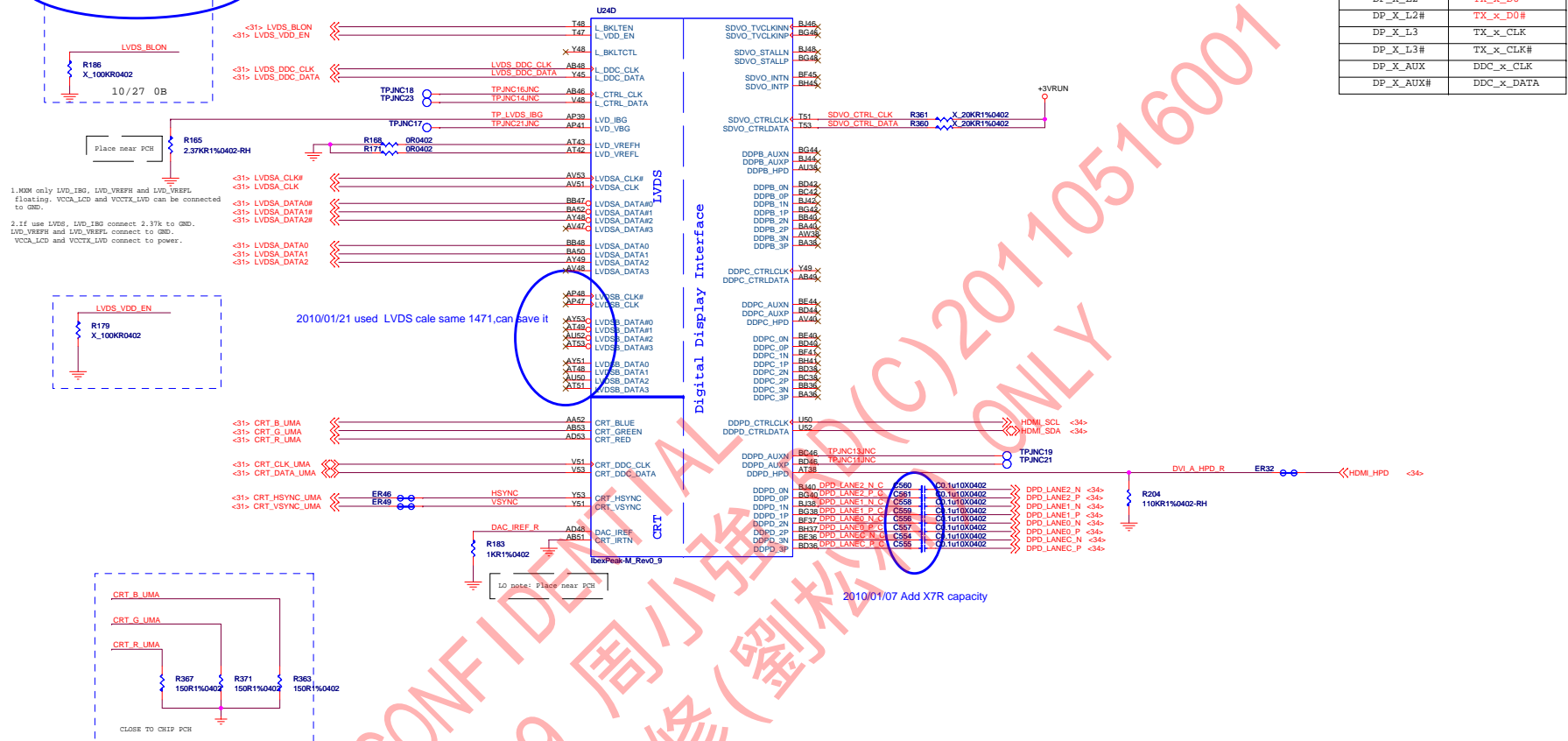
Sym	Parameter	Min	Max	Units	Notes
t209	PWROK active to PROCWRGD active	See Note 7	—	ms	7
t206	PWROK deglitch time	1	—	ms	6

- Ensure PWROK is a solid logic '1' before proceeding with the boot sequence. Note: If PWROK drops after t206 it will be considered a power failure.
- t209 minimum timing selectable as 1 ms (recommended), 5 ms, 50 ms, or 100 ms using bits 9:8 of PCHSTRP15.

2010/01/22 modify value from 1.1K to 10K

2010/01/22 remove component to save layout space

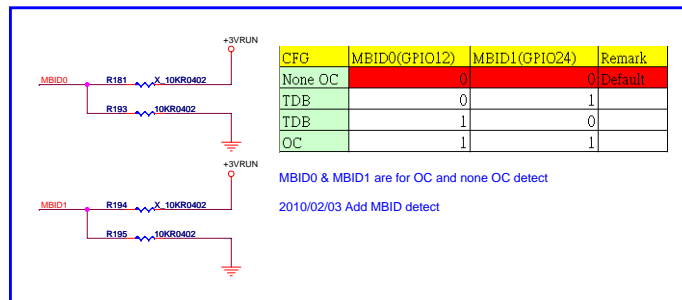
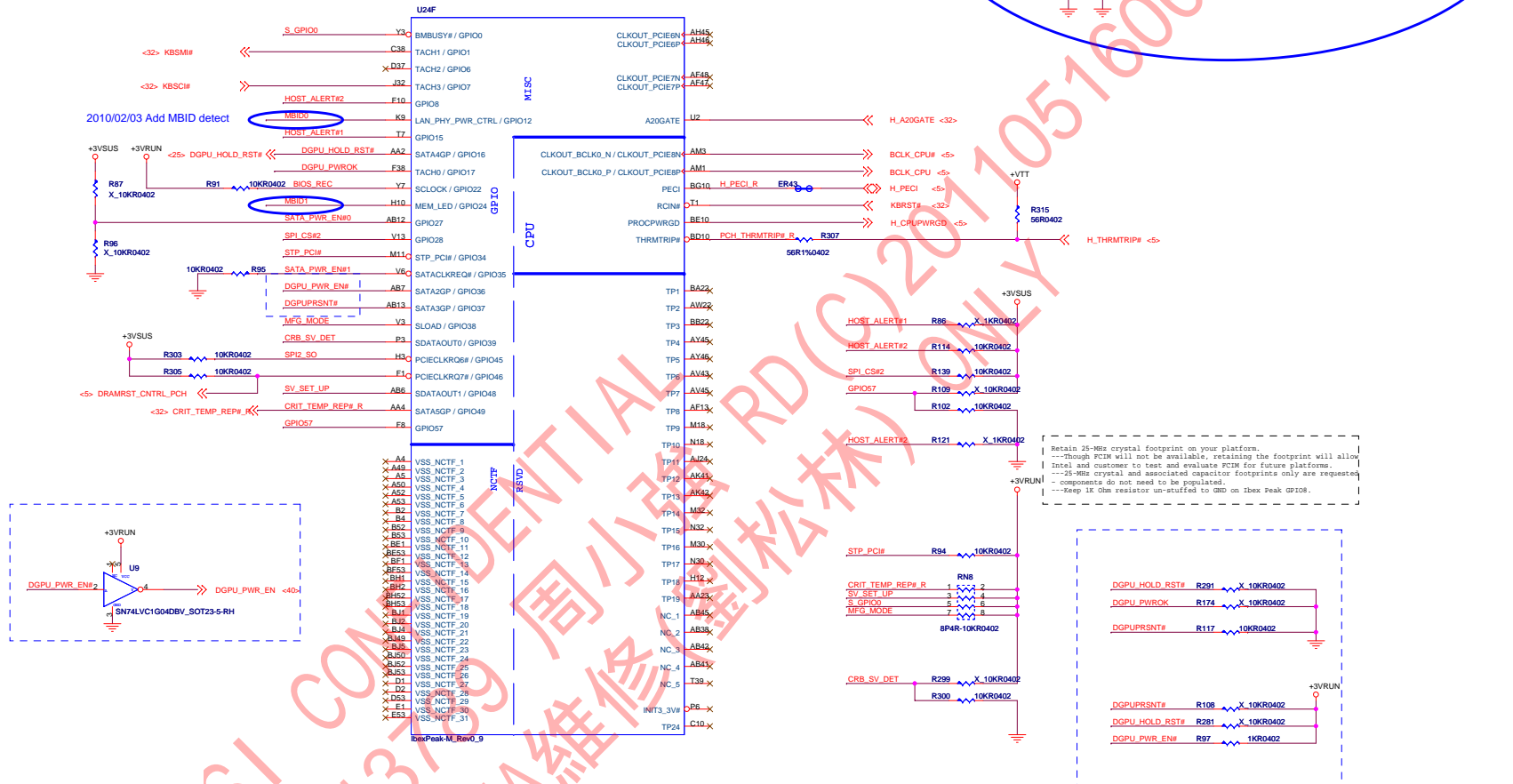
## IBEXPEAK - M (LVDS,DDI)



CONFIDENTIAL (C) 20170516001  
60013789 周小強 (羅松)  
FOR RMA維修



## IBEXPEAK - M (GPIO,VSS\_NCTF,RSVD)





**Table 8-4. Measured I/O voltage rails**

Voltage Rail	Voltage (V)	Source
V_CPU_IO	1.1/1.05	50
V5REF	5	
V5REF_Sus	5	
Vcc3_3	3.3	
VccADAC	3.3	
VccADPLL	1.05	
VccADPLLB	1.05	
VccCore	1.05	
VccDMI	1.1	
VccIO	1.05	
VccLAN	1.05	
VccME	1.05	
VccME3_3	3.3	
VccpNAND	1.8	
VccRTC	3.3	
VccSus3_3	3.3	
VccSusHDA	3.3	
VccVRM	1.8/1.5	
VccALVDS	3.3	
VccTX_LVDS	1.8	

SKU	Thermal Design Power (TDP)	Notes
QM57	3.5 W	1
HM57	3.5 W	1
HM55	3.5 W	1
PM55	3.5 W	1
QS57	3.4 W	1

Voltage Rail	Voltage (V)	S0 Iccmax Current Integrated Graphics (A)	S0 Iccmax Current External Graphics (A)	S0 Idle Current Integrated Graphics (A)	S0 Idle Current External Graphics (A)	Sx Iccmax Current (A)	Sx Idle Current (A)	G3
V_CPU_IO	1.1/1.05	.001	.001	.001	.001			—
V5REF	5	.001	.001	.001	.001			—
V5REF_Sus	5	.001	.001	.001	.001	.001		—
Vcc3_3	3.3	.305	.305	.0176	.0176			—
VccADAC	3.3	.075	.0011	.0011	.0011			—
VccADPLL	1.05	.088	.0176	.825	.0044			—
VccADPLLB	1.05	.088	.0176	.0044	.0044			—
VccCore	1.05	1.43	1.254	.3685	.2805			—
VccDMI	1.1	.055	.055	.0011	.0011			—
VccIO	1.05	3.23	2.628	.463	.285			—
VccLAN	1.05	.220	.220	.066	.066	.132		—
VccME	1.05	1.2	1.2	.186	.186	.98	.0044	—
VccME3_3	3.3	.031	.031	.0022	.0022	.0154	.0022	—
VccpNAND	1.8	.0055	.0055	.0022	.0022			—
VccRTC	3.3	.0011	.0011	.0011	.0011	.0011	.0011	6 uA See notes 1, 2
VccSus3_3	3.3	.087	.087	.0132	.0132	.133	.0297	—
VccSusHDA	3.3	.0088	.0088	.001	.001	.001	.001	—
VccVRM	1.8/1.5	.156	.114	.113	.045			—
VccALVDS	3.3	.0011	.0011	.0011	.0011			—
VccTX_LVDS	1.8	.066	.0011	.0198	.0011			—



## IBEXPEAK - M (GND)



## Intel® 5 Series Chipset Mobile SKUs

Feature Set	SKU Name(s)				
	QM57	HM57	PM55	HM55	QSS7
PCI Express* 2.0 Ports	8	8	8	6 <sup>5</sup>	8
USB* 2.0 Ports	14	14	14	12 <sup>4</sup>	14
SATA Ports	6	6	6	4 <sup>6</sup>	6
HDMI/DVI/VGA/SDVO/DisplayPort	Yes	Yes	No	Yes	Yes
LVDS	Yes	Yes	No	Yes	Yes
Graphics Support with PAVP 1.5	Yes	Yes	No	Yes	Yes
FIS Based Port Multiplier Support	Yes	Yes	Yes	No	Yes
Intel® Quiet System Technology	No	No	No	No	No
Intel® Rapid Storage Technology	AHCI	Yes	Yes	Yes	Yes
	Raid 0/1/5/10 Support	Yes	Yes	Yes	No
Intel® ME Ignition FW only	No	No	Yes	No	No
Intel® AT	Yes	Yes	No	Yes	Yes
Intel® AMT 6.0	Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Business	Yes	No	No	No	Yes
Intel® Remote PC Assist Technology for Consumer	No	Yes	No	No	No
Intel® Remote Wake Technology	No	No	No	No	No

Figure 2-6. Platform Power Block Diagram—S3, M-Off, with WoL, No WoWLAN

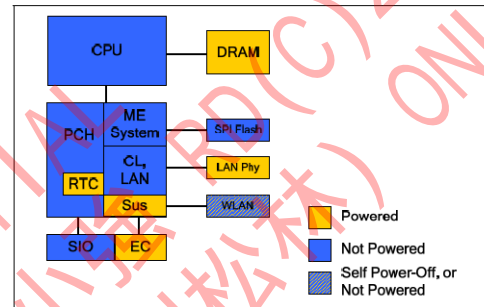


Figure 2-9. Platform Power Block Diagram—S4-S5, M-Off, with WoL, No WoWLAN

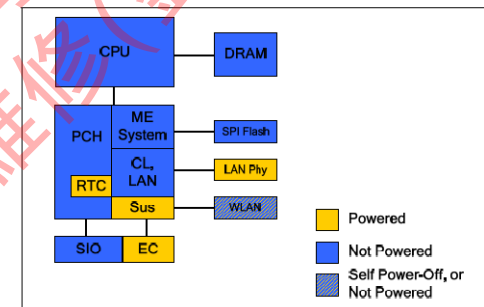
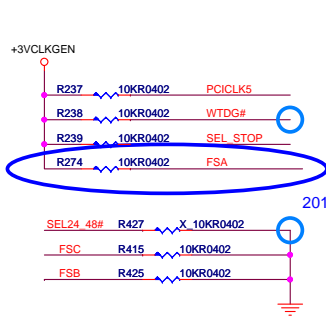


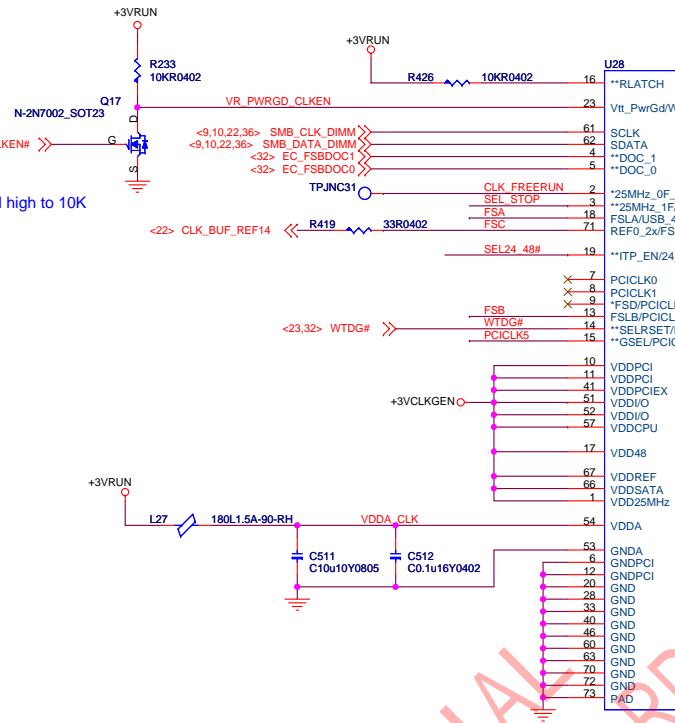
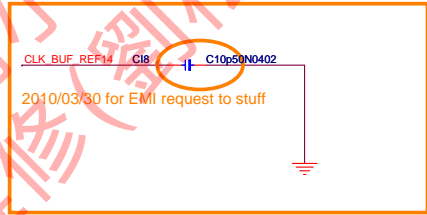
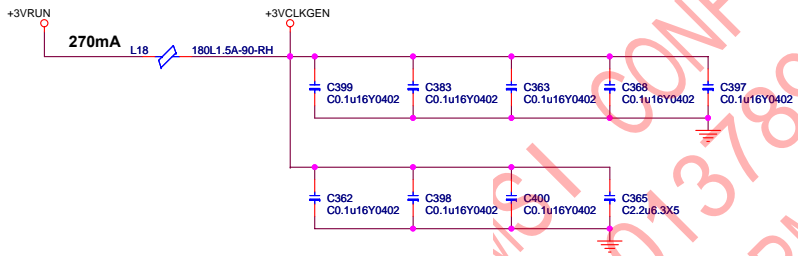
Table 113. Power Delivery Summary for Intel Management Engine SubSystem (Sheet 1 of 2)

What It Powers	Rail	Sx <sup>1</sup> /M3	Sx/Moff <sup>2</sup>	Sx/Moff/WOL <sup>3</sup>	Source	Enabled By	Power OK indicator
Platform 5-V Rail	V5.0A	On	On	On	5 V Always (5x)		
DRAM VDD	V1.5U	On in S3	On in S3	On in S3	V1.5U	SLP_S4#	
DRAM VTT	V0.75S or V0.75U	Off <sup>4</sup>	Off <sup>4</sup>	Off <sup>4</sup>	V0.75S or V0.75U	SLP_S3#	
CK50S	3.3 CK50S	Off <sup>5</sup>	Off <sup>5</sup>	Off <sup>5</sup>	V3.3S	CKPWRGD	
Mobile Intel® 5 Series Chipset	1.05 VCORE	Off <sup>5</sup>	Off <sup>5</sup>	Off <sup>5</sup>	V1.05S		PWROK
WLAN	V3.3A	On	On	On	3.3 V Always		
M3 Support + Intel® 82577 GbE LAN							
Intel® ME Local RAM	V1.05M	On	Off	Off	V1.05M	SLP_M# <sup>6</sup>	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	On	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	On	Off	Off <sup>7</sup>	V3.3M	SLP_M# <sup>6</sup>	MEPWROK
Integrated LAN controller	VCCLAN	On	Off	Off	V1.05M	SLP_M# <sup>6</sup>	
No M3 Support + Intel® 82577 GbE LAN							
Intel ME Local RAM	V1.05M	Off	Off	Off	V1.05M	SLP_M# <sup>6</sup>	MEPWROK
PHY LAN	V3.3M_WOL V1.1_LAN_M	Off	Off	On	V3.3M V1.05M	SLP_LAN#	
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off <sup>7</sup>	V3.3M	SLP_M# <sup>6</sup>	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	V1.05M	SLP_M# <sup>6</sup>	
No M3 Support + No Intel® 82577 GbE LAN							
Intel ME Local RAM	V1.05M/1.1M	Off	Off	Off	V1.05M	SLP_M# <sup>6</sup>	MEPWROK
SPI Flash PCH SPI Interface	V3.3M_SPI	Off	Off	Off <sup>7</sup>	V3.3M	SLP_M# <sup>6</sup>	MEPWROK
Integrated LAN Controller	VCCLAN	Off	Off	Off	Grounded		

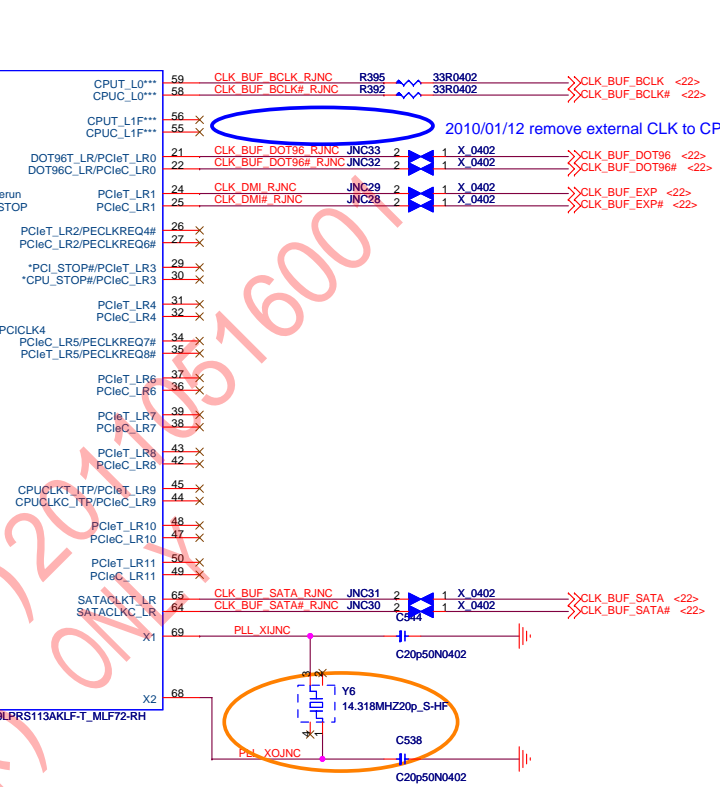


2010/01/22 modify pull high to 10K

- Pin 3 (SEL\_STOP)**  
1 = Selects pin 29/30 to be PCI\_STOP#/CPU\_STOP#  
0 = Selects pin 29/30 to be PCIeX outputs
- Pin 14 (RESET)**  
1 = RESET\_IN#/RESET#  
0 = PCICLK4 output
- Pin 15 (GSEL)**  
1 = Selects DOT 96Mhz  
0 = Selects PCIeX0/ 3.3V PCI clock output
- Pin 19 (ITP\_EN/24\_48MHz)**  
1 = CPU\_ITP



2010/01/07 Add for EMI request



2010/03/22 modify Y6 PN to D04-0103000-F07 and C load form 22p to 20p

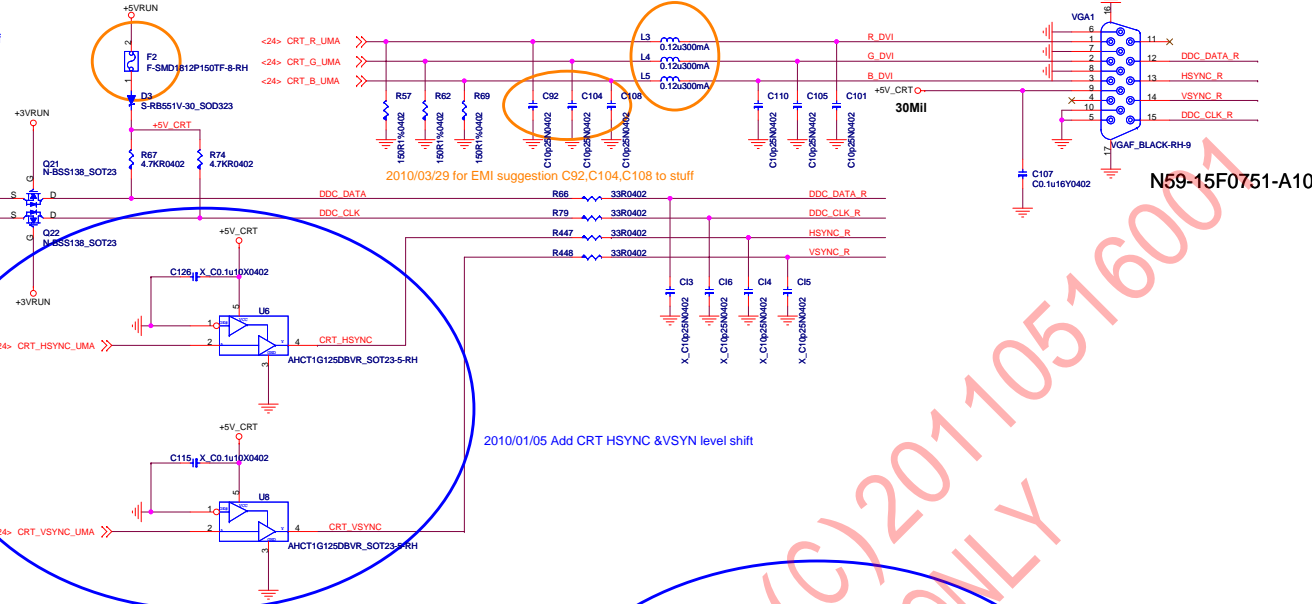
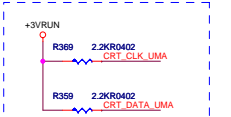
MICRO-STAR INT'L CO.,LTD.			
Title			
Clock Generator (ICS9LPR113)			
Size	Document Number	Rev	
Custom	MS-1481	0B	
Date:	Thursday, April 08, 2010	Sheet	30 of 56

# CRT

2010/03/07 Add fuse for safety request(near Connector)

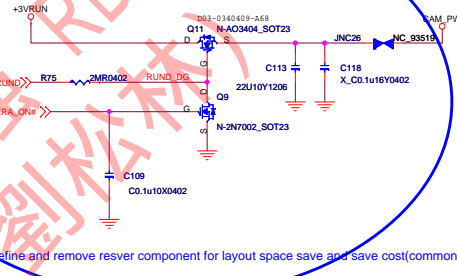
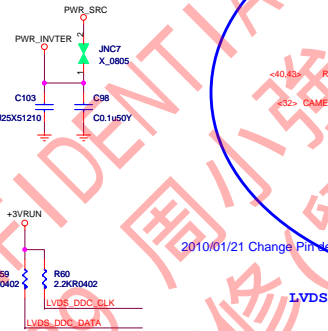
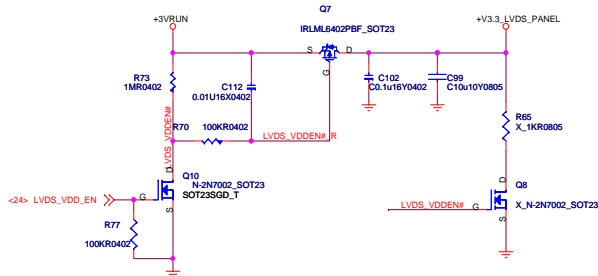
2010/03/29 for EMI suggestion modify bead to inductor 120nH

2010/01/22 modify R369,R359 to stuff

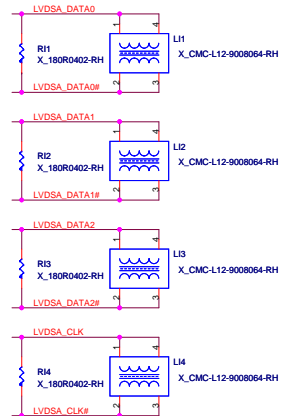


N59-15F0751-A10

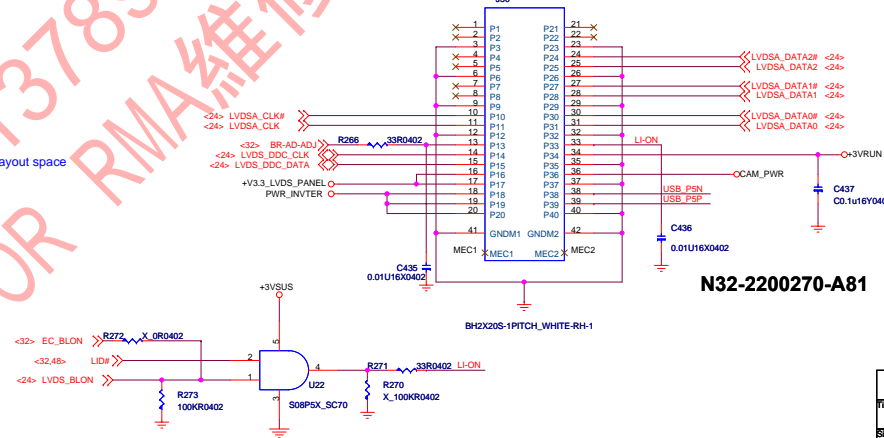
# LVDS



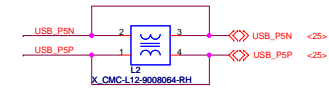
2010/01/21 Change Pin define and remove reser component for layout space save and save cost(common used 1471 LVDS cable)

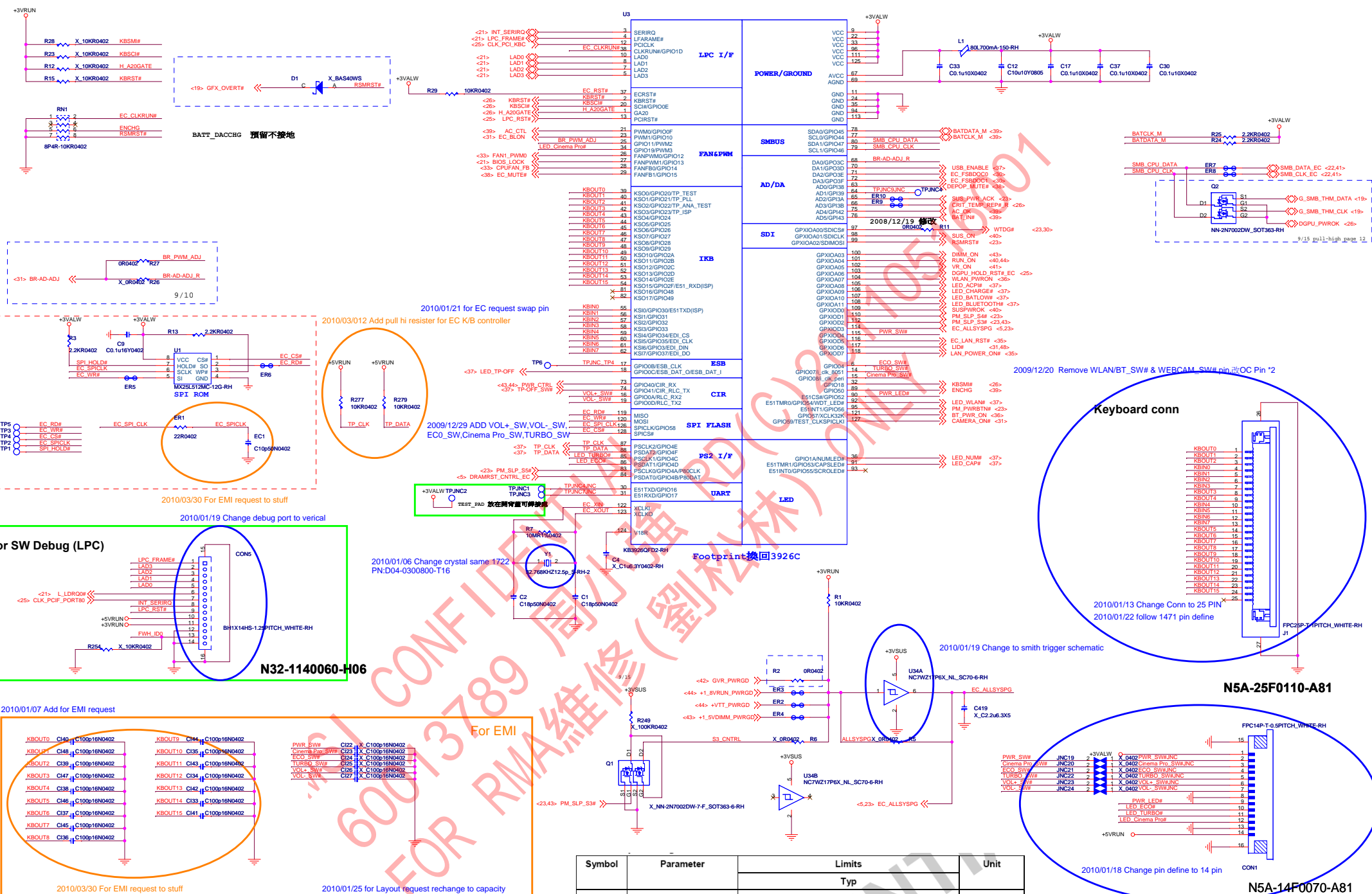


2010/01/21 remove reser component for layout space



N32-2200270-A81

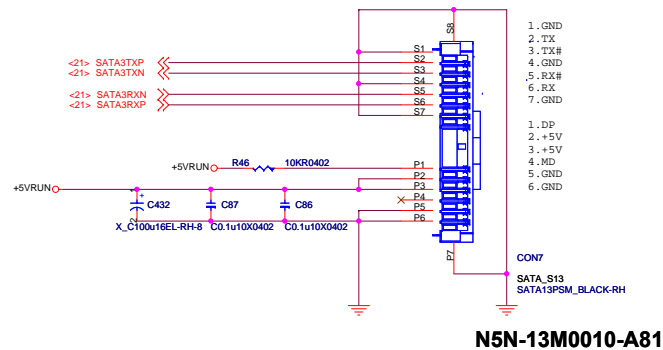




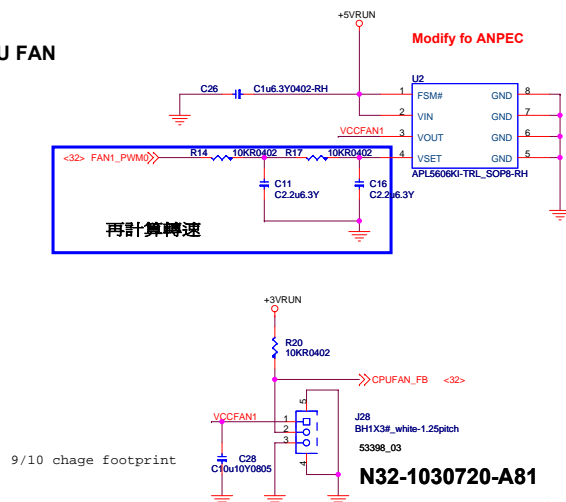
Symbol	Parameter	Limits	Unit
		Typ	
Icc	Typical current consumption in operating state under Windows environment. All clock domains are running, and no keyboard/mouse activities.	20	mA



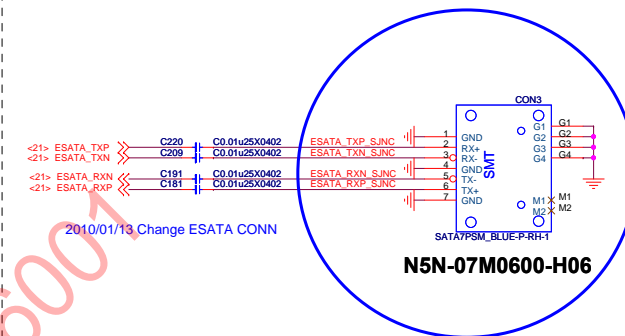
## SATA ODD



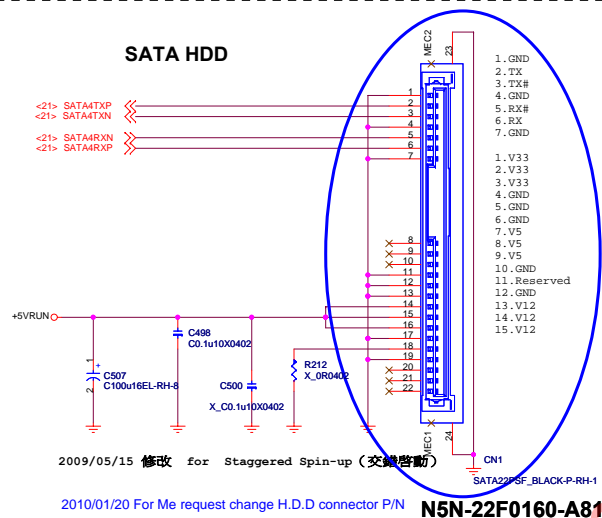
## CPU FAN



## ESATA

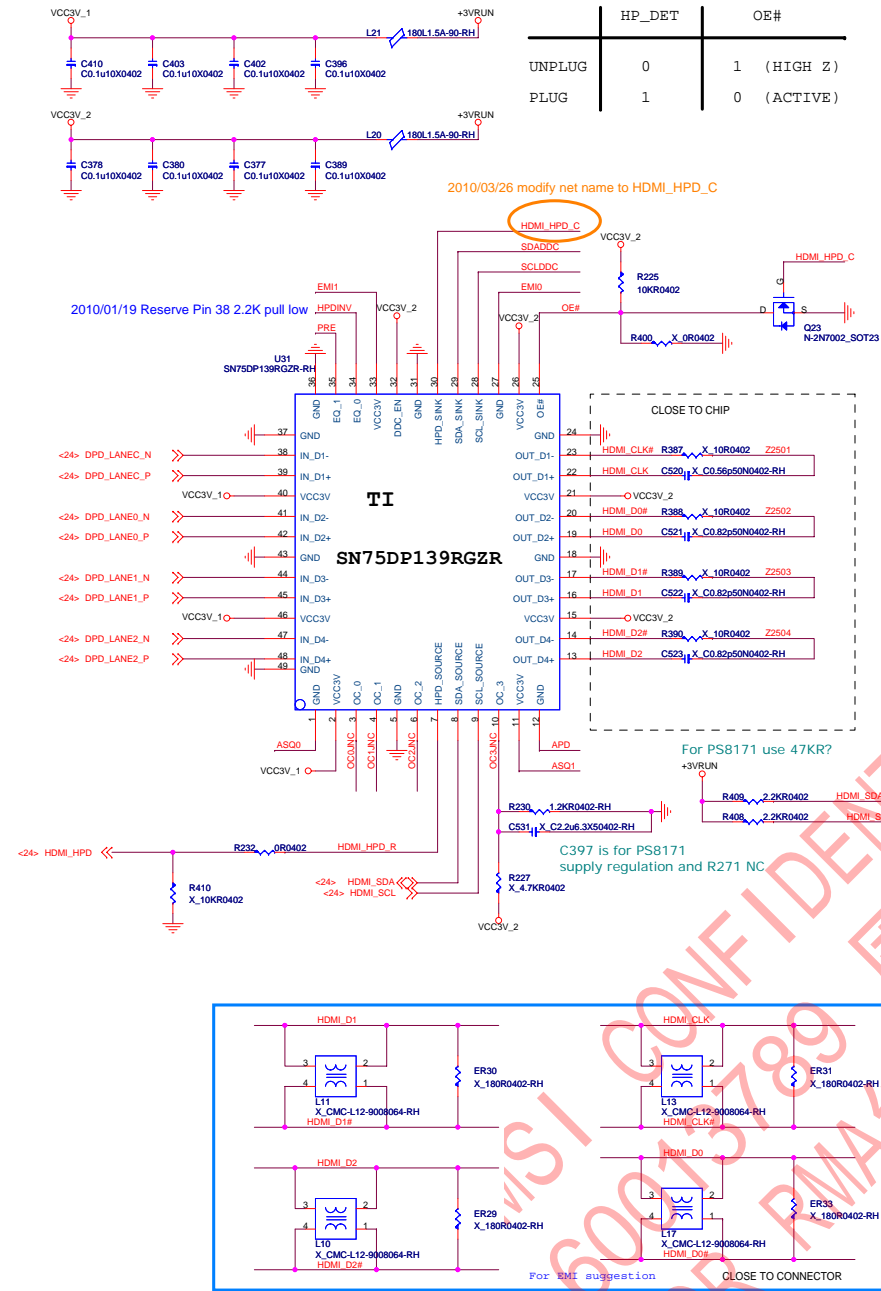


## SATA HDD

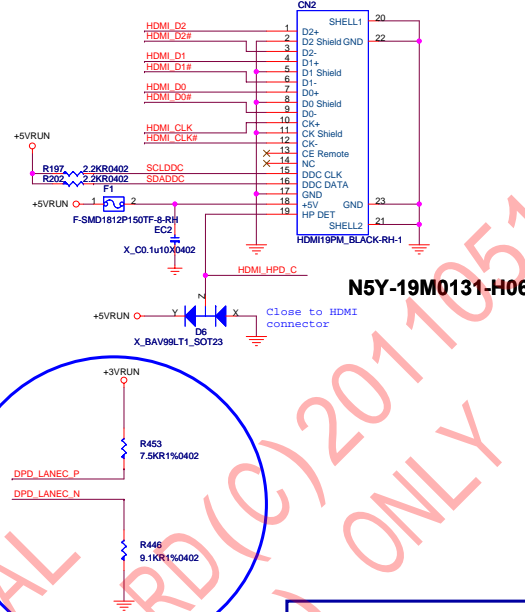


MSI MICRO-STAR INT'L CO.,LTD.			
Title			
ODD,HDD,ESATA,FAN			
Size	Document Number	Rev	
Custom	MS-1481	05	
Date:	Sheet	33	of 56

# HDMI Switch

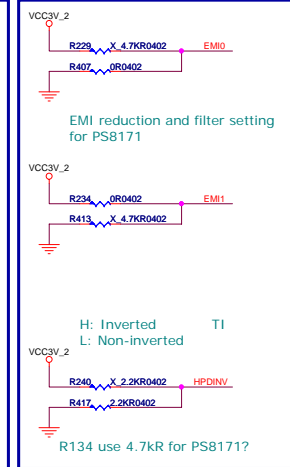
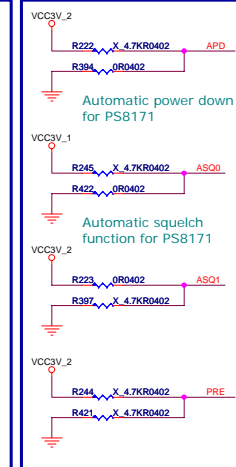
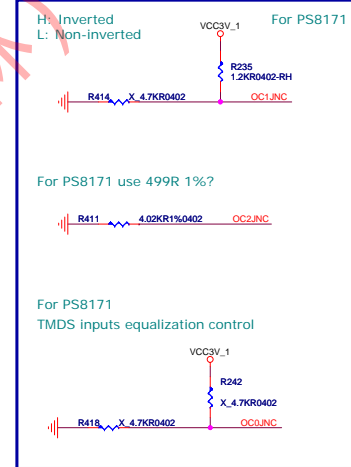


## HDMI connector



SN75DP139	PS8171	Pin no.
Floating	TMDS inputs equalization control (internal pull-down~500KΩ) PEQ = LOW: Mid level EQ (Default) PEQ = HIGH: High level EQ PEQ = MID: Low level EQ	Pin 3
High	(Internal pull down~500KΩ) PIO = LOW: HPD = HPD_SINK @ 3.3V CMOS output PIO = High: HPD= HPD_SINK# (inverted HPD) @ 0.9V	Pin 4
GND	[AS01,AS00] = HL: No automatic squelch (Internal pull down~500KΩ) LL: Automatic squelch enable, Level = 120mVpp, default timer LH: Automatic squelch enable, Level = 100mVpp, default timer HH: Automatic squelch enable, Level = 80mVpp, default timer ML: Automatic squelch enable, Level = 120mVpp, extended timer MH: Automatic squelch enable, Level = 100mVpp, extended timer LM: Automatic squelch enable, Level = 80mVpp, extended timer HM: Reserved MM: Reserved	Pin 1 Pin 11
4.65K to GND	499R to GND	Pin 6
GND	Automatic power down management (Internal pull up~500KΩ) APD = LOW: Automatic power down disable APD = HIGH: Automatic power down enable APD = MID: Reserved	Pin 12
1.2K to GND	2.2uF to GND	Pin 10
GND	EMI reduction and filter setting. (EMI1 internal pull up~500KΩ; EMI0 internal pull down~500KΩ) [EMI1,EMI0] = HL: No EMI reduction EMI0 = HIGH: Reduced rise/fall time MID: Reduced rise/fall time, 2nd EMI1 = LOW: EMI filter setting 1 MID: Reserved	Pin 27 Pin 33
Note2	DDC Active Buffer enable and setting (internal pull-down~500KΩ) DDCBUF = LOW: No DDC active buffer, passive DDC level shifting DDCBUF = HIGH: Active DDC buffer enable, setting 1 DDCBUF = MID: Active DDC buffer enable, setting 2	Pin 34
Floating	TMDS output driver pre-emphasis level setting (internal pull down~500KΩ) PRE = LOW No pre-emphasis PRE = HIGH: Low level pre-emphasis is added PRE = MID: High level pre-emphasis is added	Pin 35

Note2: High is HPD logic inverted, Low is HPD logic non-inverted



Note: add 0.1u cap at each power pin of LAN, please don't save.

2010/03/03 modify CHOKE1 form 2.2uH to 4.7uH for Realtek request

Use External 1.05V Supply When Disable Switch Regulator.  
If Using External 1.2V Supply Pls. Contact With FAE.

2010/01/08 remove it, if used jump write

For RTL8105E

\* C1841 to C1844 are for VDD10 pins-- 3, 13, 29, 45.

For RTL8111E

\* C1841 to C1848 are for VDD10 pins-- 3, 6, 9, 13, 29, 41, 45.

Part Reference

Enable Switch Regulator

Disable Switch Regulator

	Choke1	C1840	C1846	R1662	R1668
Enable Switch Regulator					
Disable Switch Regulator	X	X	X	X	X

For RTL8105E

\* C1851 to C1855 are for VDD33 pins-- 27, 39, 42, 47, 48.

For RTL8111E

\* C1851 to C1856 are for VDD33 pins-- 12, 27, 39, 42, 47, 48.

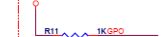
VDD33 power on rise time >1ms  
C1851 to C1856 Close To LAN chip

Remove For Disable  
Switch Regulator

## EEPROM Select

For RTL 8105E

VDD33



2.When using EFuse/BIOS Patch.

FOR RTL 8111E

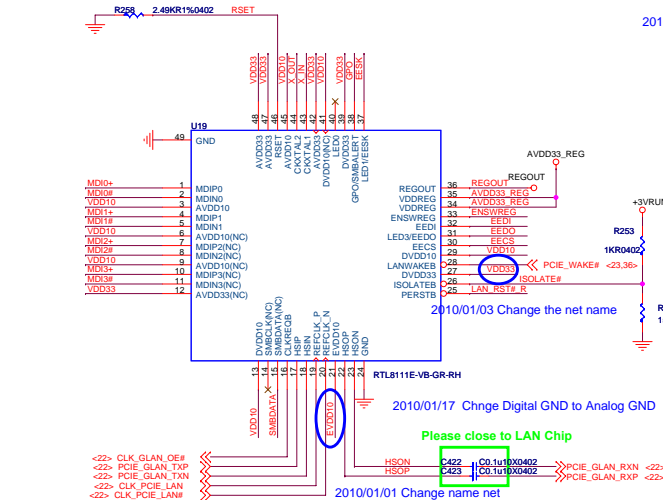
VDD33



3.When using EFuse/BIOS Patch without ASF function.

## For EMI

2010/03/26 reserve 0.1uF \*4 for EMI



2010/01/03 Change the net name

2010/01/17 Chng Digital GND to Analog GND

Please close to LAN Chip

2010/01/01 Change name net

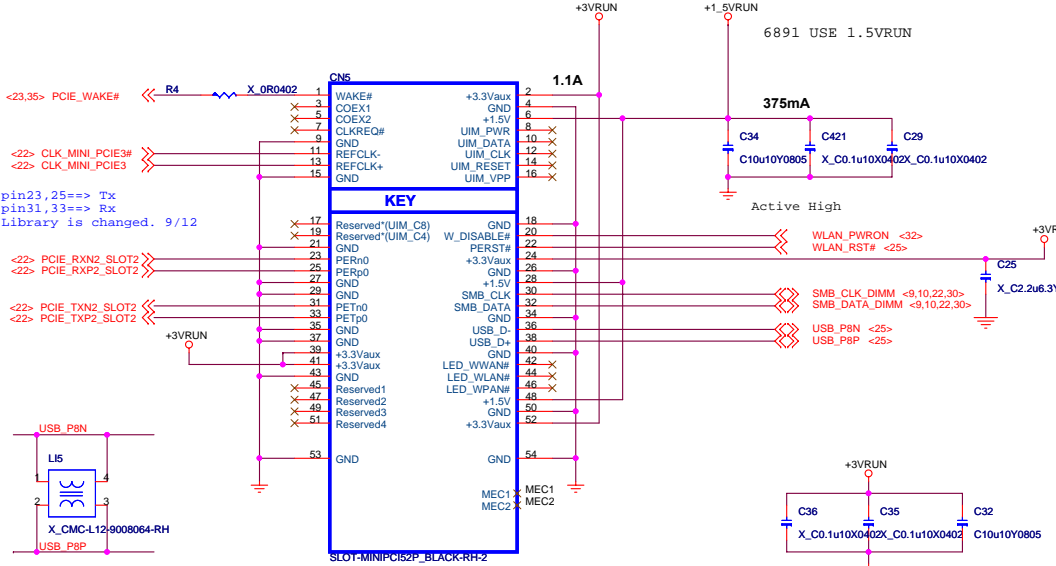
2010/01/22 Add for LAN ECO

2010/01/03 follow reference schematic remover 3 capacity

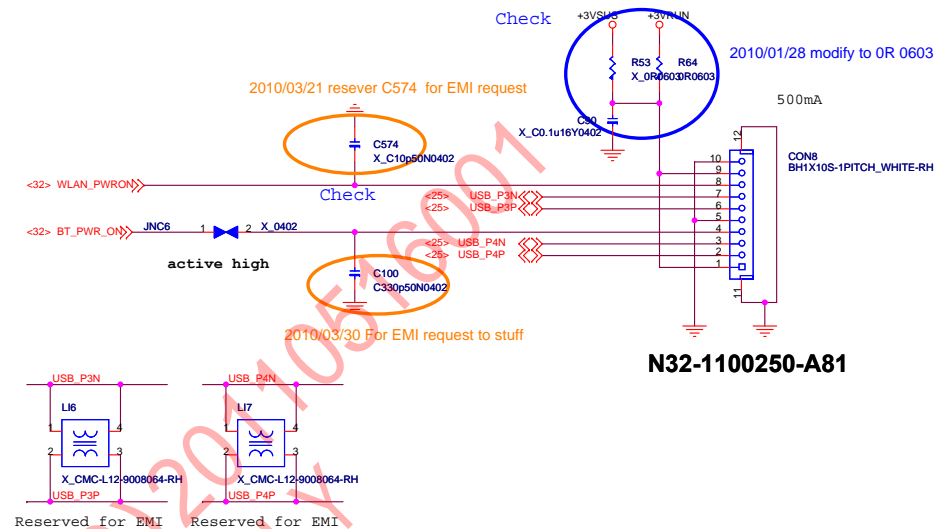
2010/01/04 follow reference schematic add 10K pull low

N55-08F0491-SH4

# WLAN CARD



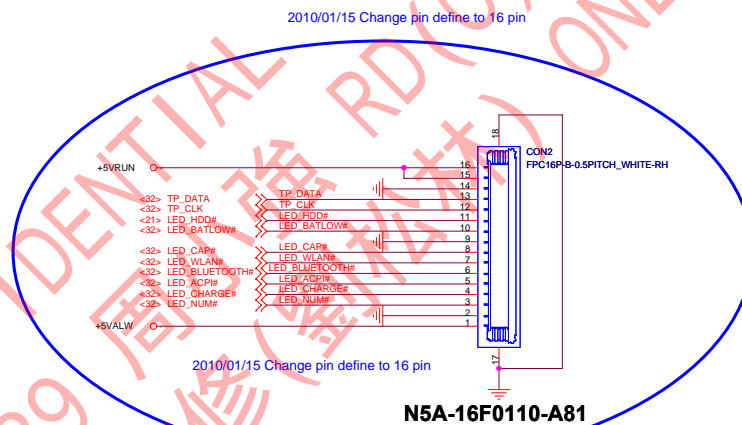
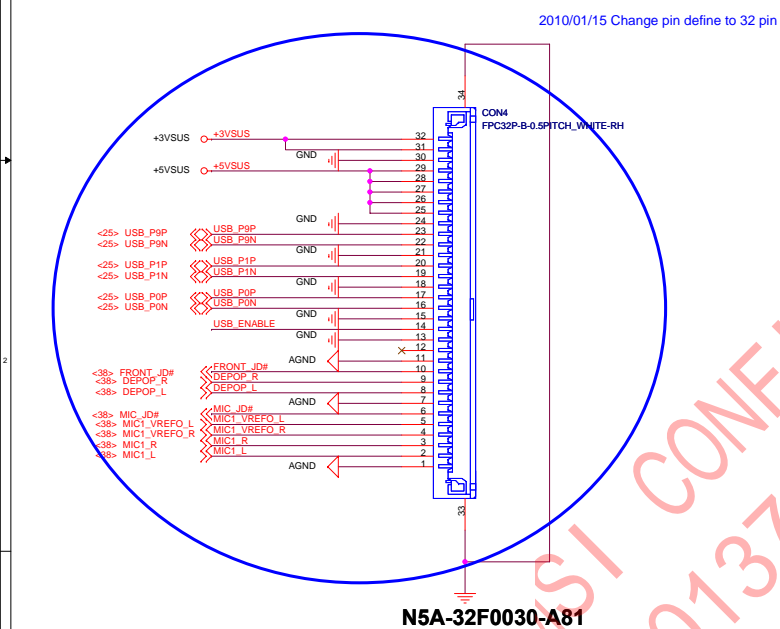
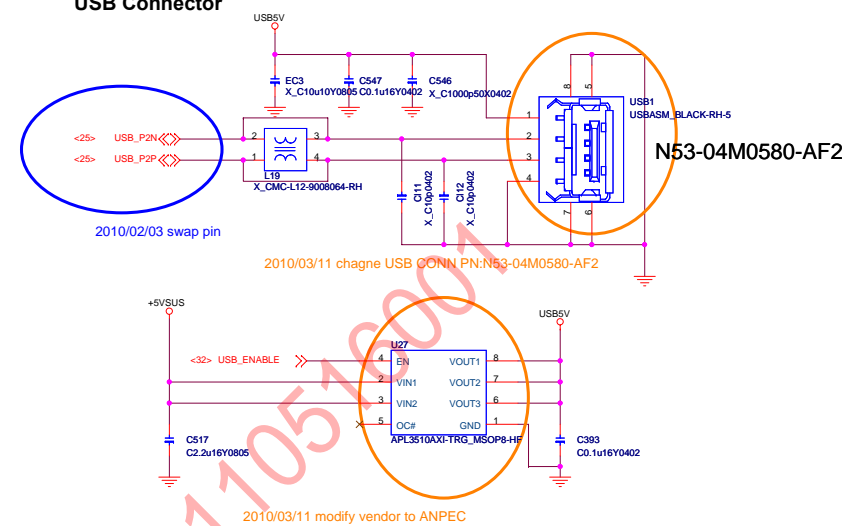
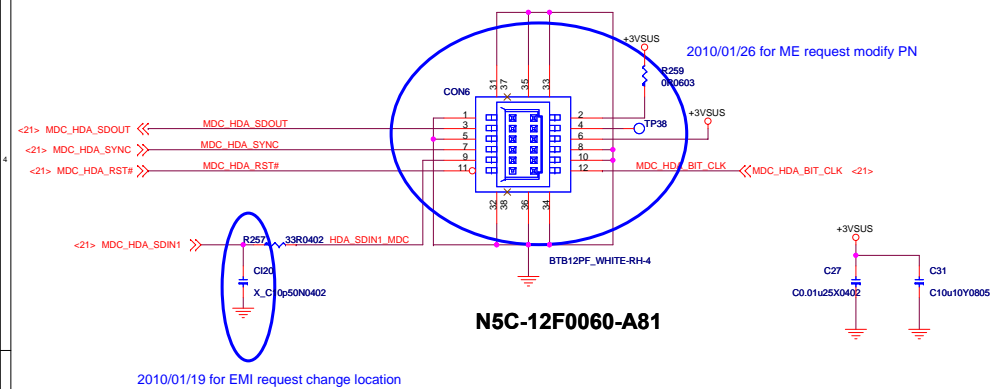
# MS-3871 BT & WLAN COMBO



N32-1100250-A81

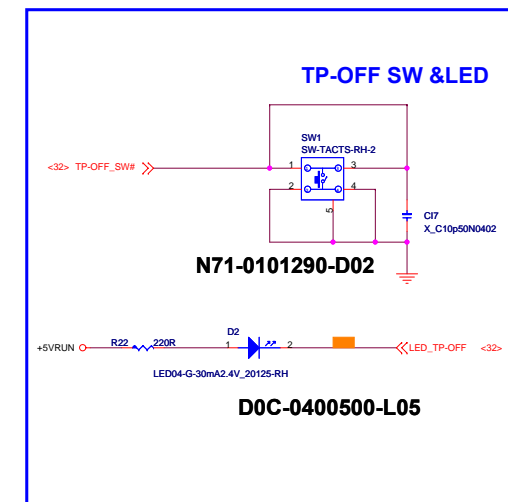
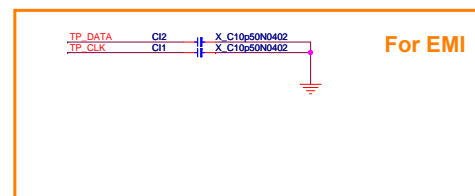
MDC

USB Connector



Connector to P.46 Board C

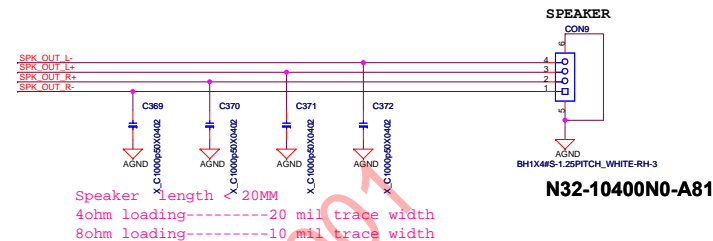
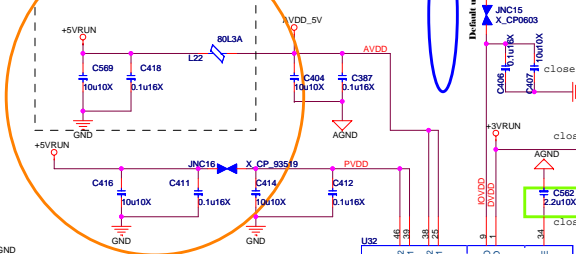
Connector to P.44 Board A



2010/03/07 Change C569,C416,L22,C416,C411 to stuff

2009/12/29 Delete +1.5V RUN

FOR ALC269-VB have internal LDO



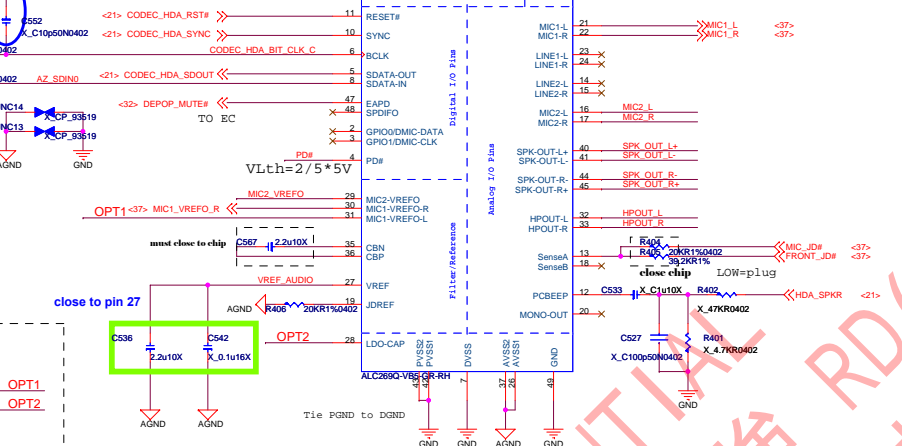
N32-10400N0-A81

Speaker length < 20MM  
4ohm loading-----20 mil trace width  
8ohm loading-----10 mil trace width

2010/01/07 change from 22p to 10 for EMI request

2010/01/07 change from 22p to 10 for EMI request

2010/01/07 change from 22p to 10 for EMI request



No Co-layout VA

VB

<37> MIC1\_VREF0\_L

AGND

close to pin 27

C536

2.2u10X

AGND

C542

0.1u16X

AGND

AGND

AGND

AGND

AGND

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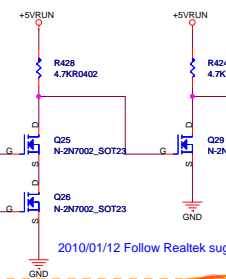
simple MUTE

No Co-layout VA

FROM EC

<32> EC\_MUTE#

<21> CODEC\_HDA\_RST#

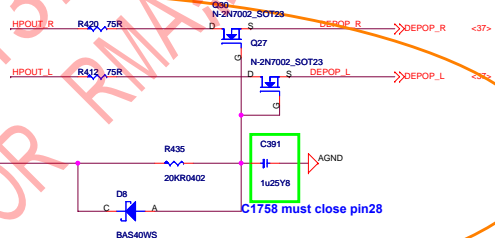


2010/01/12 Follow Realtek suggestion change schematic

For No DEPOP Stuff



2010/03/26 0B version for DEPOP stuff

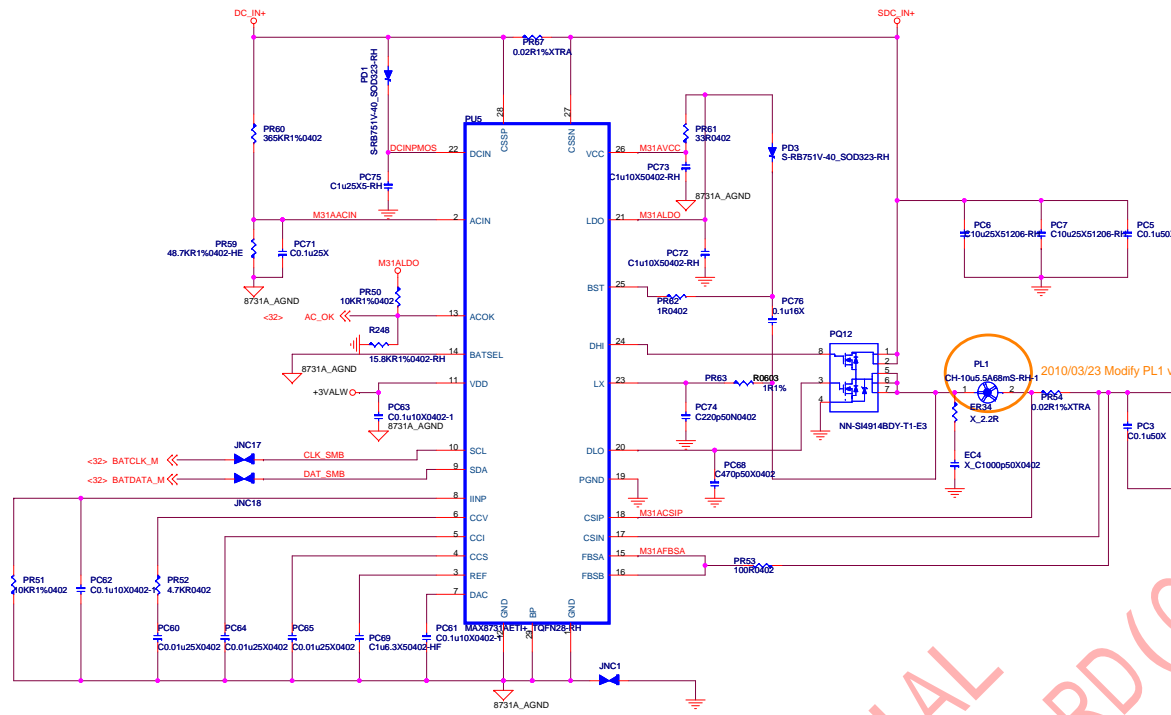


NOT STUFF

DEPOP CIRCUIT

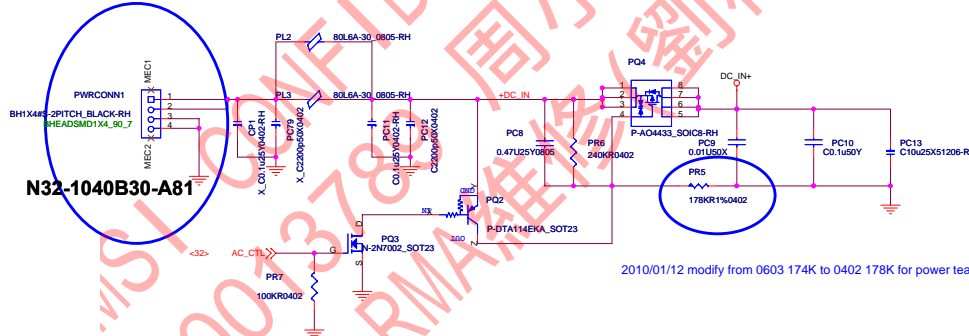


Adapter input voltage set 19 Voltage

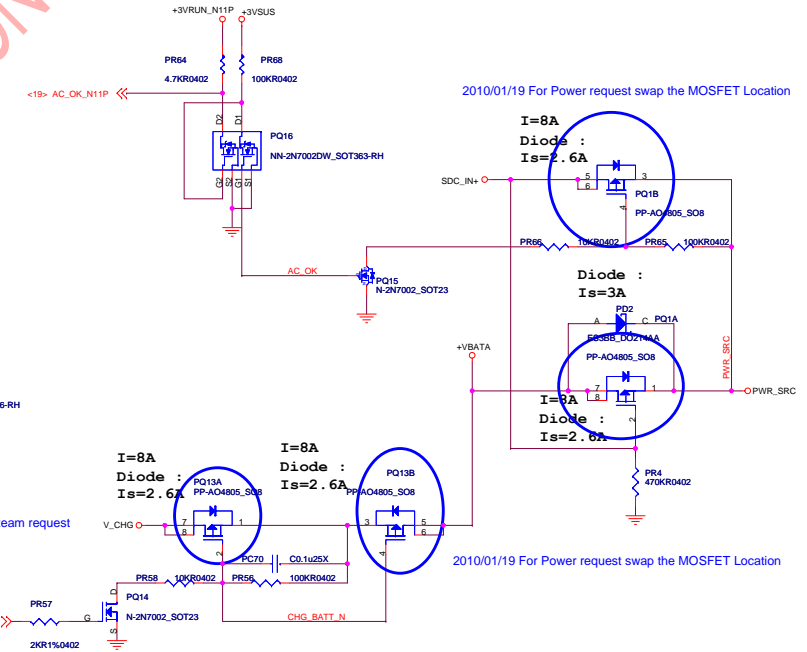


IINP :  
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.  
2.  $V\_IINP = IINP \times RS1 \times 3mA/V \times PR25$

2009/12/31 更換power connector  
2010/01/12 Chage connector same the 16G1

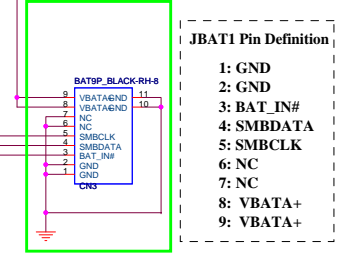


2010/01/12 modify from 0603 174K to 0402 178K for power team request



2010/01/19 For Power request swap the MOSFET Location

12/15 Change Battery Conn.

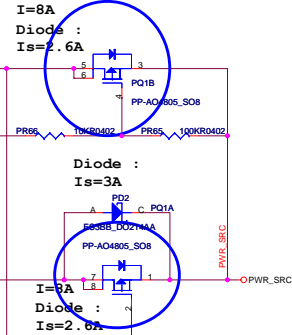


JBAT1 Pin Definition  
1: GND  
2: GND  
3: BAT\_IN#  
4: SMBDATA  
5: NC  
6: NC  
7: NC  
8: VBATA+  
9: VBATA+

N91-09M0071-AF2

2010/01/12 Power team recommend remove

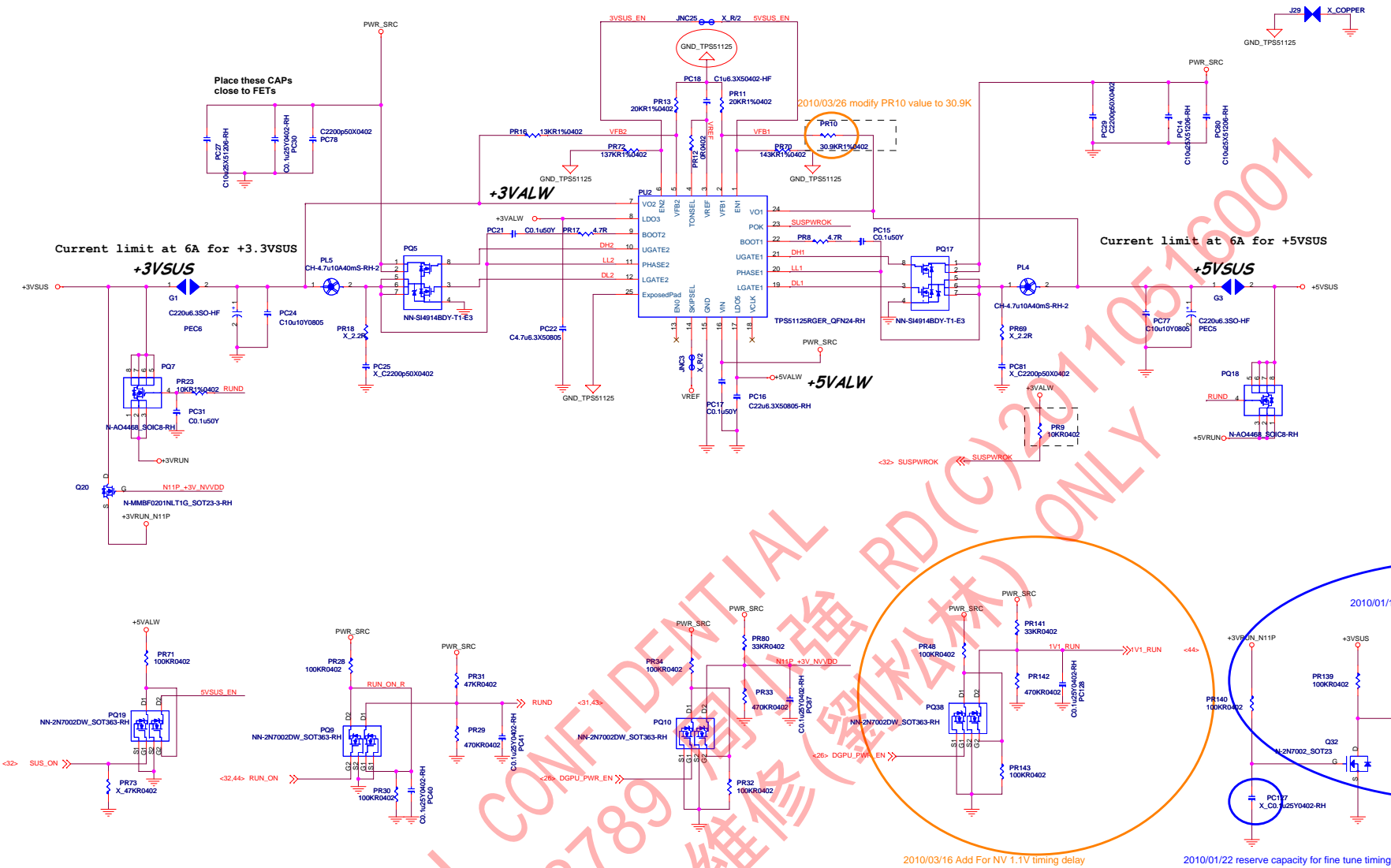
2010/01/19 For Power request swap the MOSFET Location

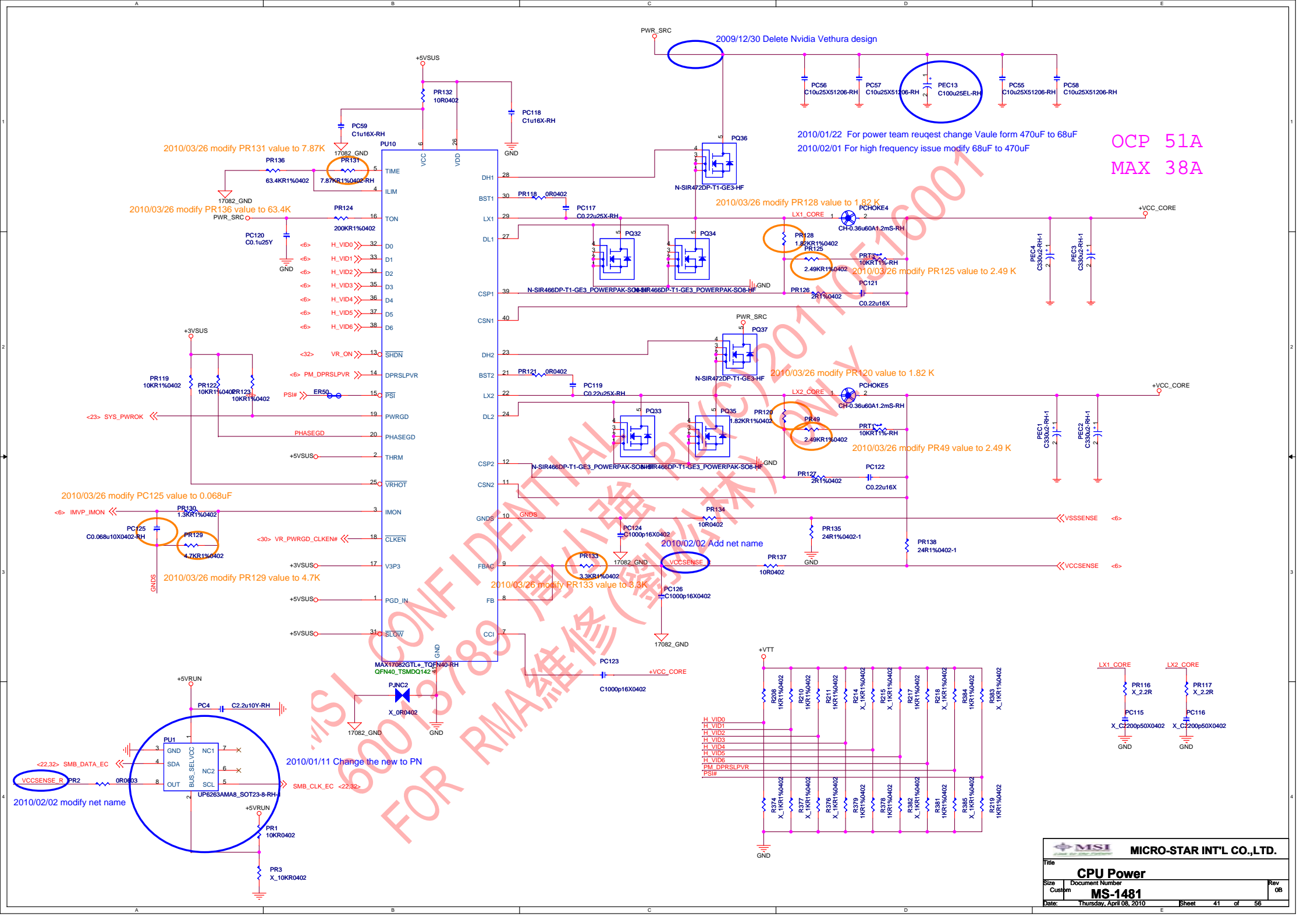


I=8A  
Diode :  
Is=2.6A

I=8A  
Diode :  
Is=3A

I=8A  
Diode :  
Is=2.6A





2010/03/26 modify PR131 value to 7.87K

2010/03/26 modify PR136 value to 63.4K

2010/03/26 modify PC125 value to 0.068uF

2010/03/26 modify PR129 value to 4.7K

2010/01/11 Change the new to PN

2010/02/02 modify net name

2009/12/30 Delete Nvidia Vethura design

2010/01/22 For power team request change Vaule form 470uF to 68uF  
2010/02/01 For high frequency issue modify 68uF to 470uF

2010/03/26 modify PR128 value to 1.82 K

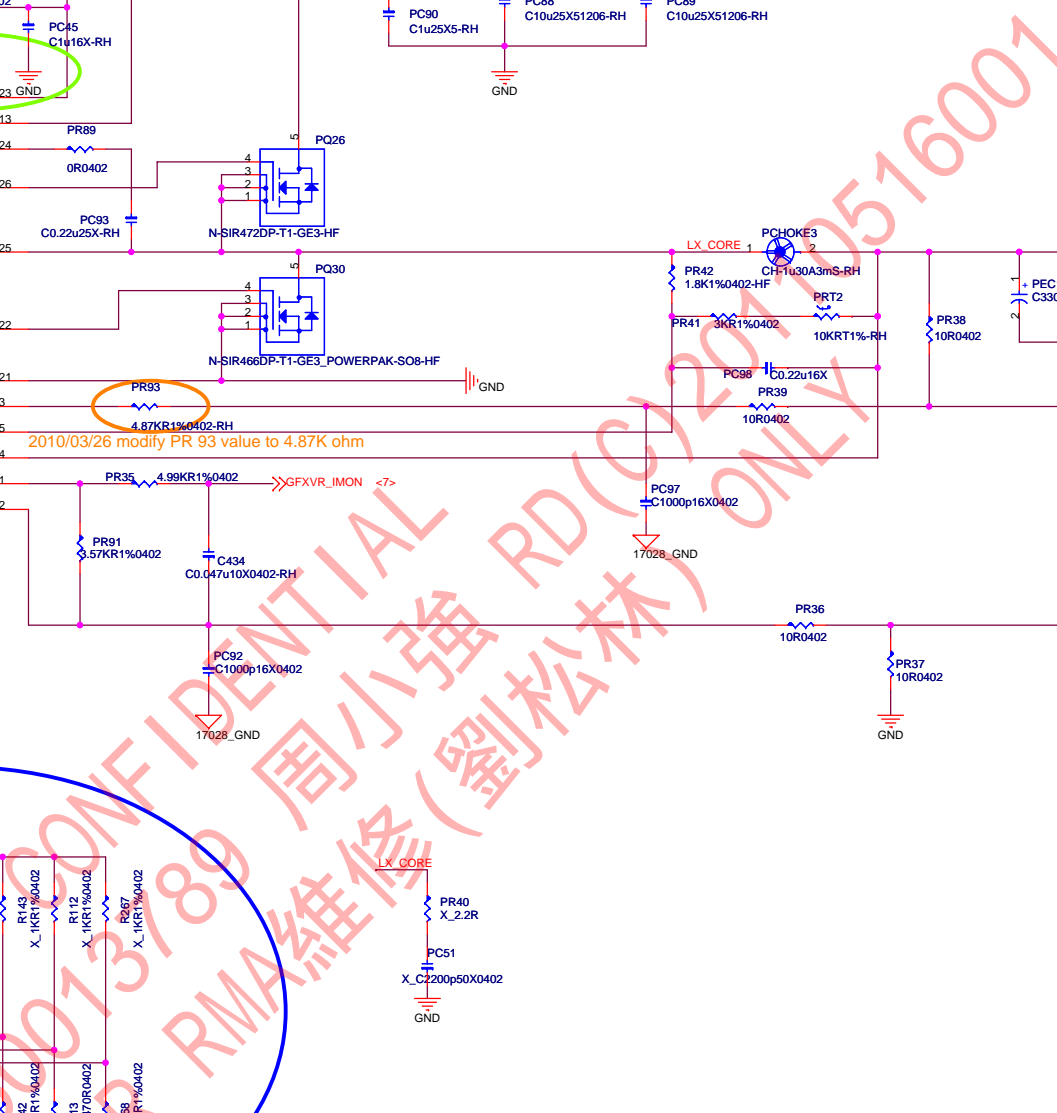
2010/03/26 modify PR120 value to 1.82 K

2010/03/26 modify PR49 value to 2.49 K

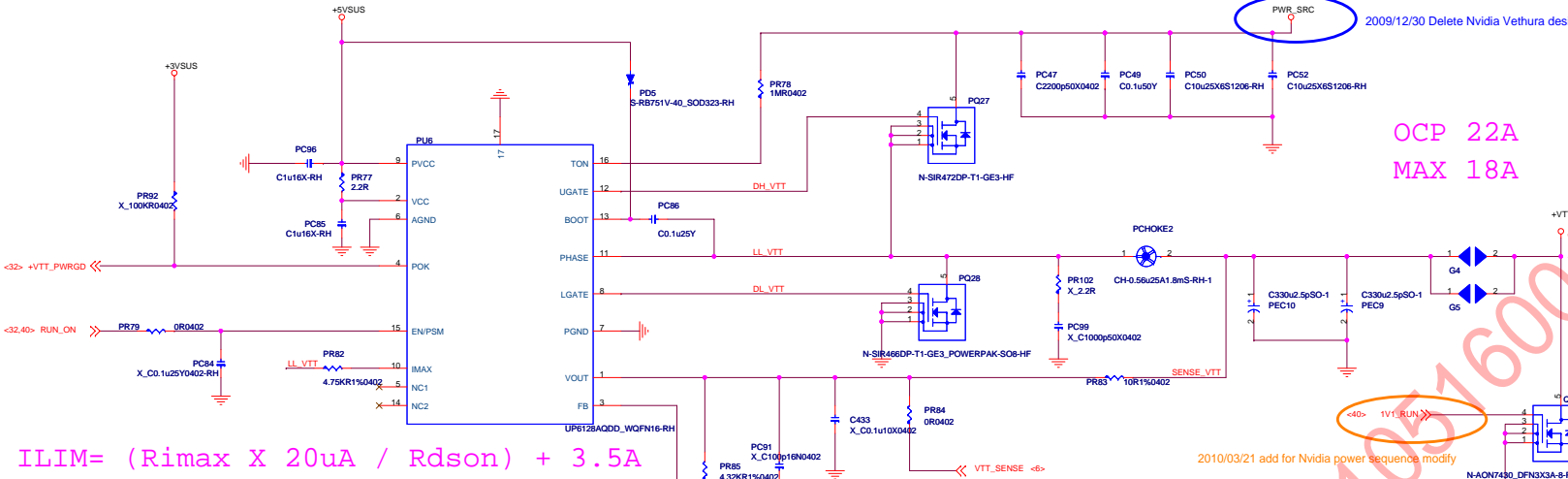
2010/02/02 Add net name

2010/03/26 modify PR133 value to 3.3K

OCP 51A  
MAX 38A

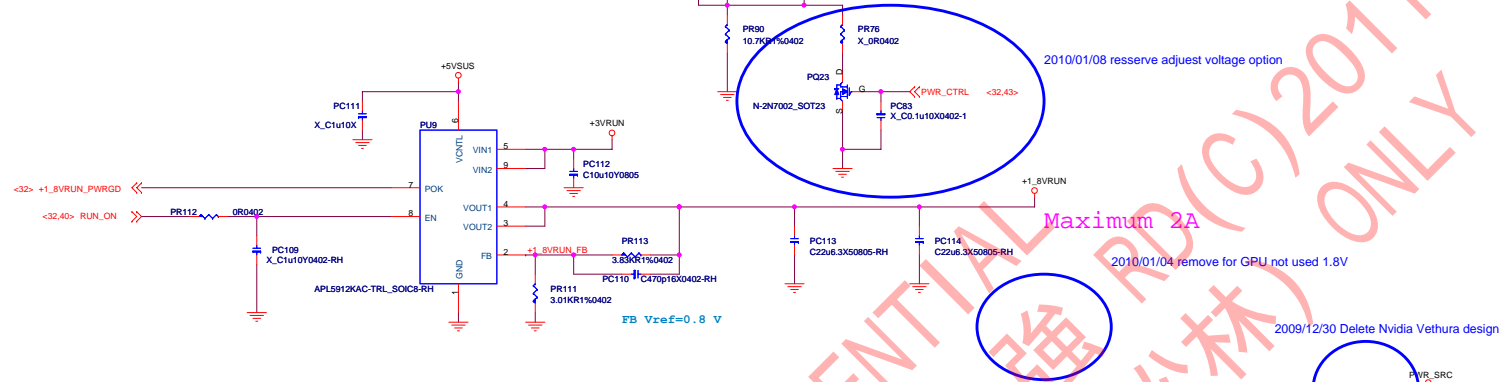




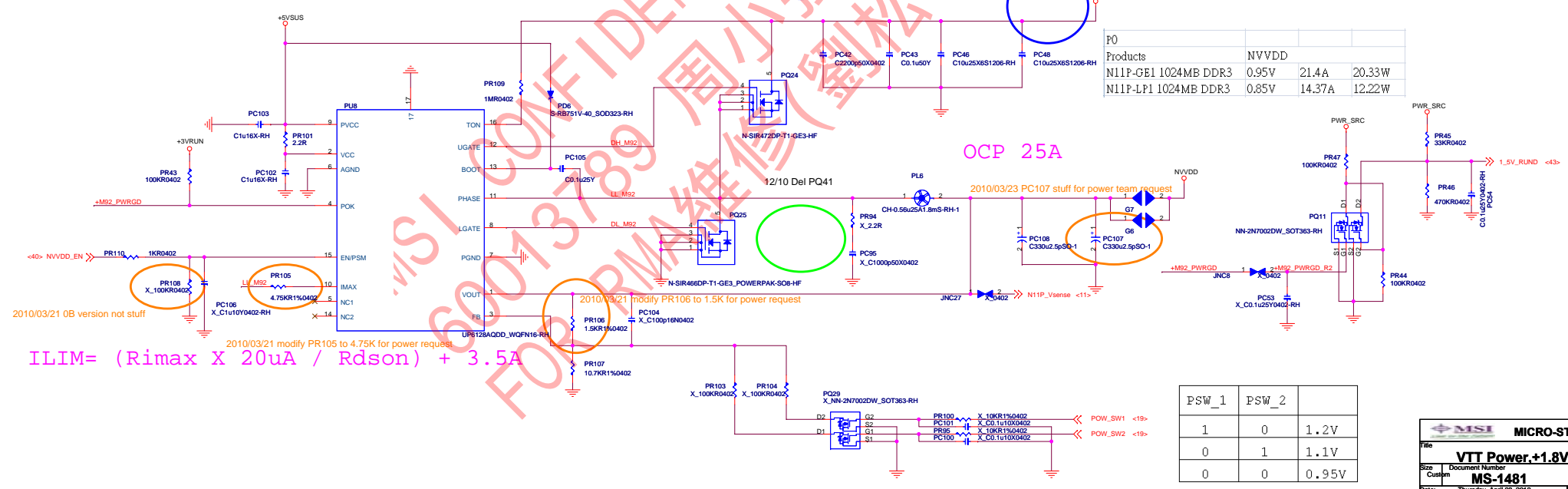


$$ILIM = (R_{imax} \times 20\mu A / R_{dson}) + 3.5A$$

P0			
Products	PCI Express 1.05V	I/O PLLVDD 1.05V	
N11P-GE1 1024MB DDR3	599.27mA	0.63W	186.77mA 0.2W
N11P-LP1 1024MB DDR3	581.74mA	0.61W	186.77mA 0.2W



P0			
Products	NVVD		
N11P-GE1 1024MB DDR3	0.95V	21.4A	20.33W
N11P-LP1 1024MB DDR3	0.85V	14.37A	12.22W



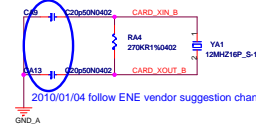
$$ILIM = (R_{imax} \times 20\mu A / R_{dson}) + 3.5A$$

PSW_1	PSW_2	
1	0	1.2V
0	1	1.1V
0	0	0.95V



# Card Reader UB6252

FOR UB6252

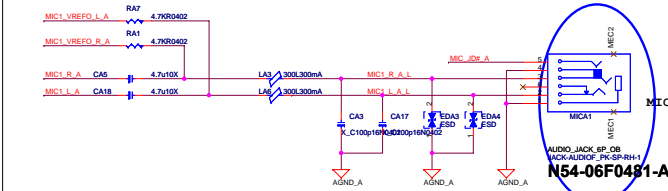
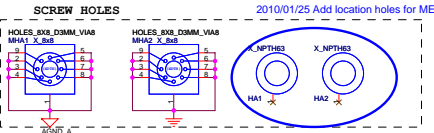


2010/01/04 follow ENE vendor suggestion change capacity to 20P

2009/12/30 Add 4.7K ohm pull hi 3V (ENE suggestion)

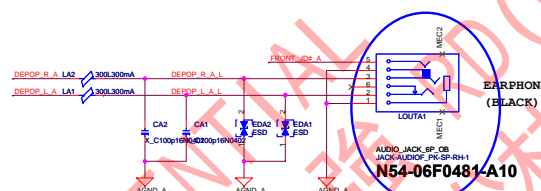
2010/01/22 modify pad size

2010/01/25 Add location holes for ME



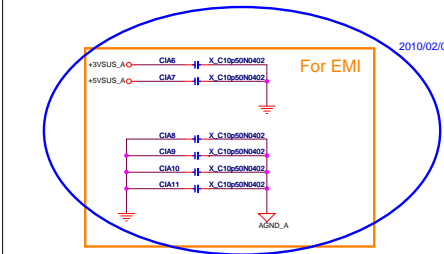
N54-06F0481-A10

2010/02/03 modify PN to N54-06F0481-A10



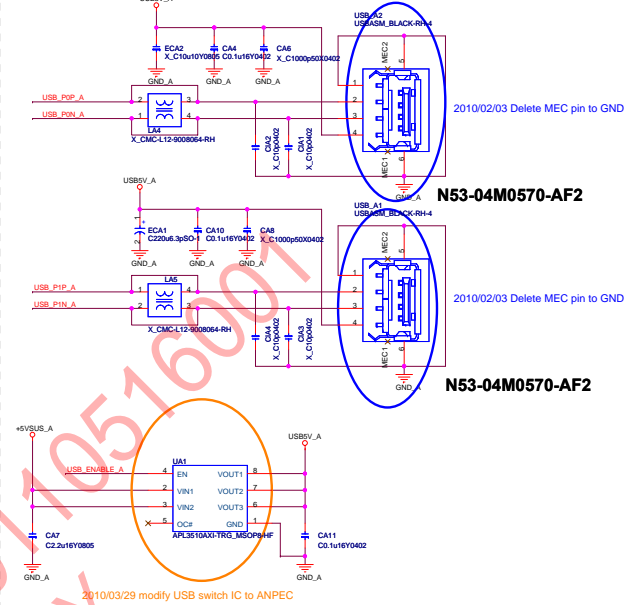
N54-06F0481-A10

2010/02/03 modify PN to N54-06F0481-A10



For EMI

2010/02/01 Reserve for EMI



2010/02/03 Delete MEC pin to GND

N53-04M0570-AF2

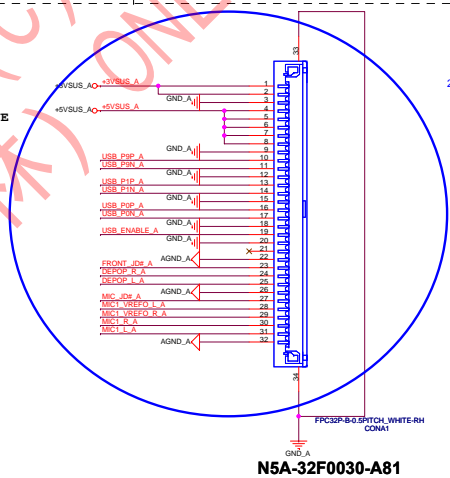
2010/02/03 Delete MEC pin to GND

N53-04M0570-AF2

2010/03/29 modify USB switch IC to ANPEC

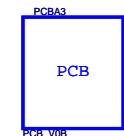


P30-1481A28-R71, 顯示規格 (標準版)  
P30-1481A28-R75, 右側 (左側/大)

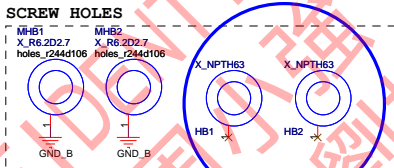
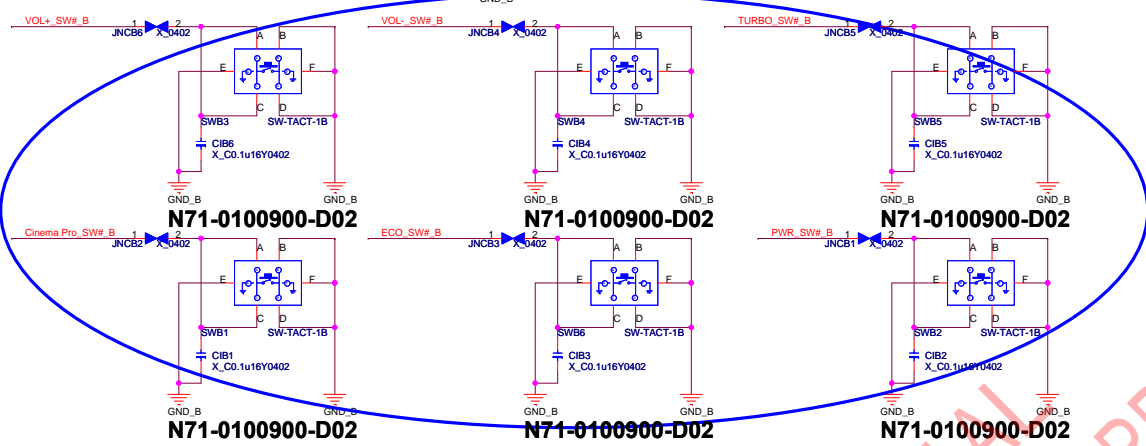


2010/01/15 Change pin define to 32 pin

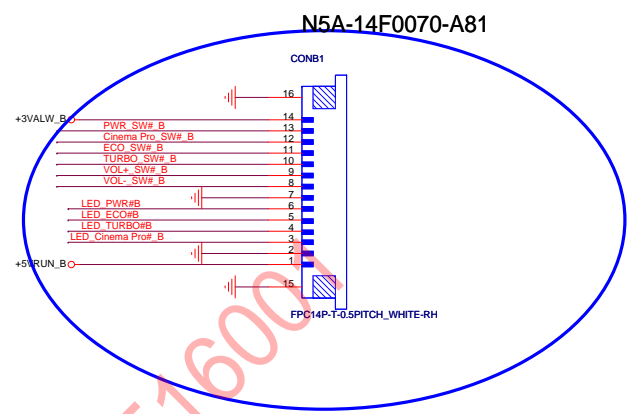
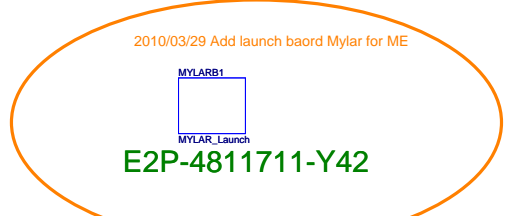
N5A-32F0030-A81



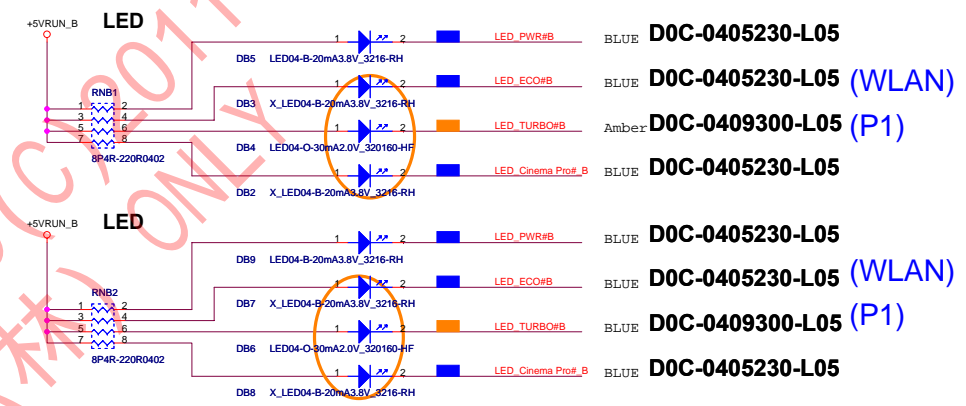
P30-1481B08-H73, 瀚手博德(薩摩亞),  
P30-1481B08-D05, 昆精(定新大陸)



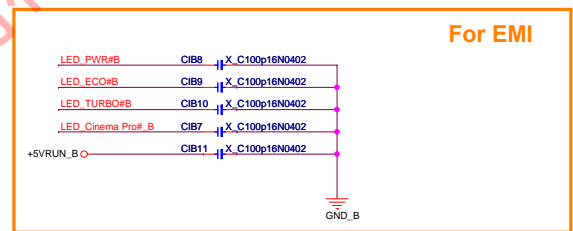
2010/01/25 Add Location holes for ME



2010/01/18 Change pin define to 14 pin

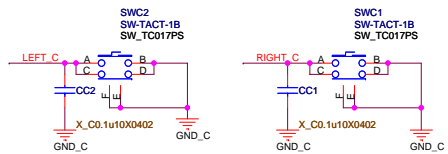


2010/03/26 modify DB4 & DB6 color to Amber  
modify DB2, DB3, DB7, DB8 to no stuff for iD request



For EMI

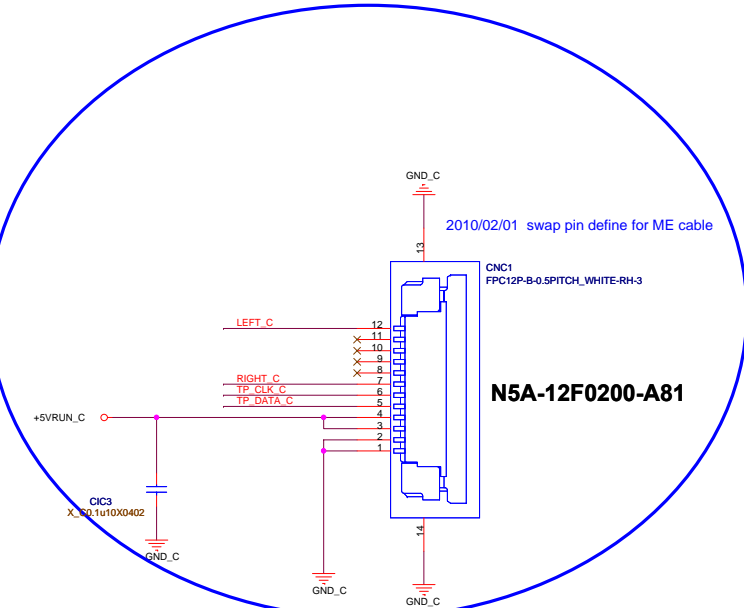
MICRO-STAR INT'L CO.,LTD.	
Launch Board	
Size	Document Number
Custom	MS-1481
Date:	Thursday, April 08, 2010
Sheet	46 of 56



**N71-0100900-D02**

**N71-0100900-D02**

2010/01/14 Chagne pin define for multi finger



2010/02/01 swap pin define for ME cable

**N5A-12F0200-A81**

For S8048D-3200 multi finger pin define



2010/03/29 Add TP board Mylar for ME

**E2P-4811811-Y42**

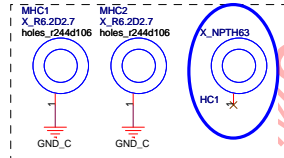
P30-1481C0B-H73, 瀚宇博德(薩摩亞)  
P30-1481C0B-D05, 昆穎(宏爾大陸)

PCBA4

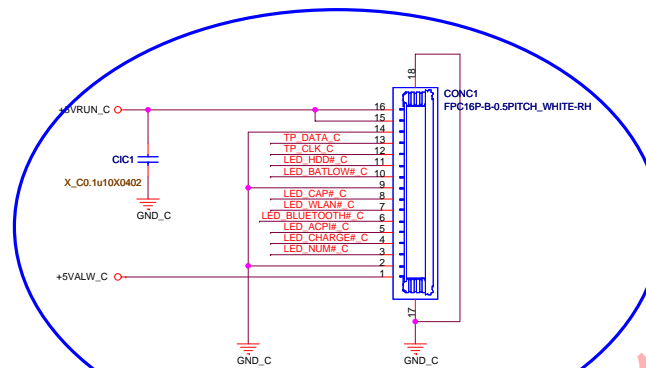
PCB

PCB\_V08

#### SCREW HOLES

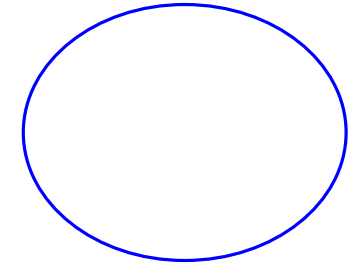


2010/01/25 Add location holes for ME

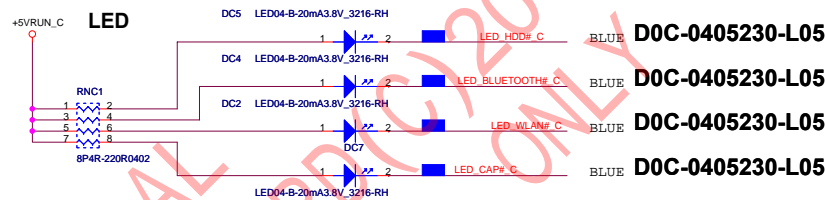


**N5A-16F0110-A81**

2010/01/15 Change pin define to 16 pin



2010/01/05 remove HDD signal MOSFET

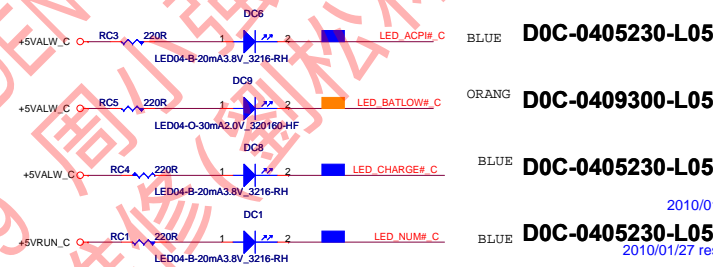


**D0C-0405230-L05**

**D0C-0405230-L05**

**D0C-0405230-L05**

**D0C-0405230-L05**



**D0C-0405230-L05**

**D0C-0409300-L05**

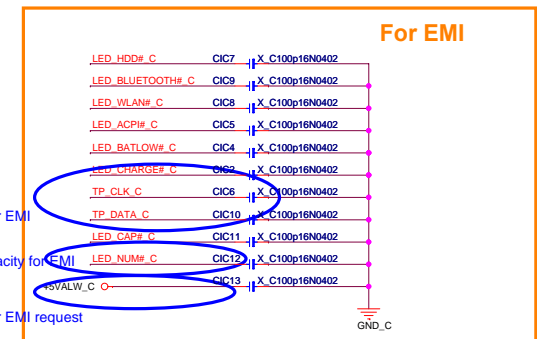
**D0C-0405230-L05**

**D0C-0405230-L05**

2010/01/26 reserve for EMI

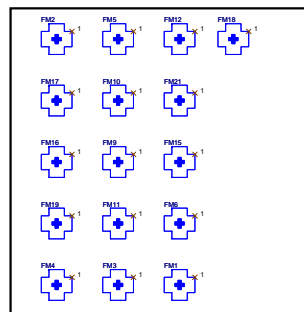
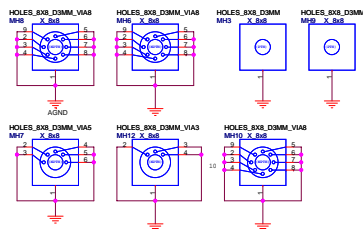
2010/01/27 reserve LED capacity for EMI

2010/02/01 reserve for EMI request

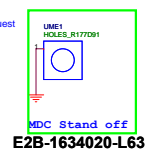
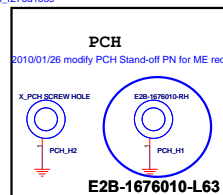
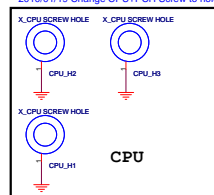


For EMI

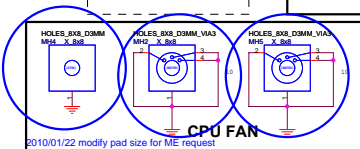
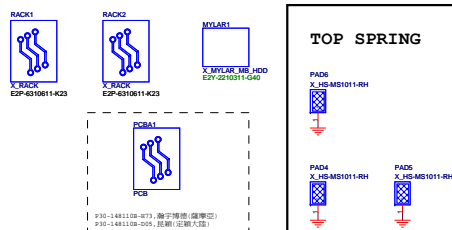
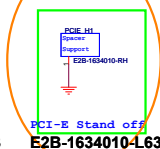
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File: <b>TP.LEDBOARD</b>	
Size: Custom	Document Number: <b>MS-1481</b>
Date: Thursday, April 08, 2010	Rev: 08
Sheet: 47	of 56



2010/01/19 Change CPU+PCH Screw to holes, /276d185s



2010/03/25 modify PN to E2B-1634010-L63 for ME request



2010/01/22 modify pad size for ME request  
2010/01/28 modify screw for EMI request

65 ohm



70 ohm



2010/03/21 0B version modify impedance test line

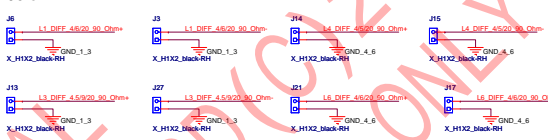
80 ohm



85 ohm



90 ohm



100 ohm



37.5 ohm



38 ohm



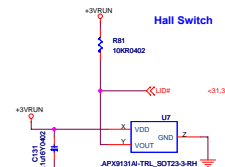
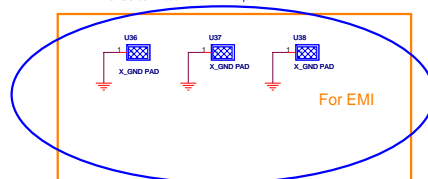
40 ohm

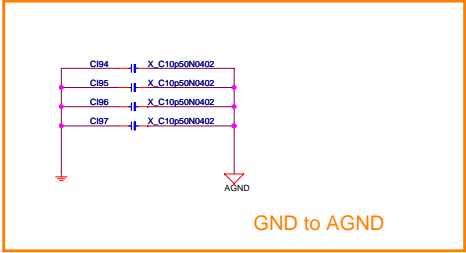
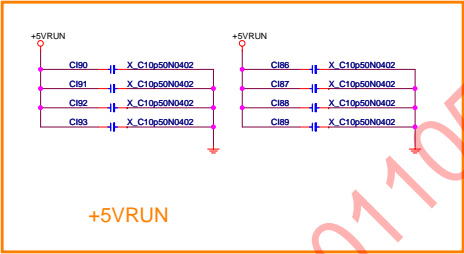
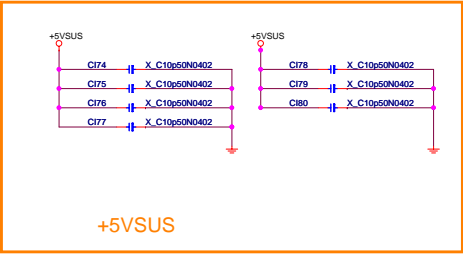
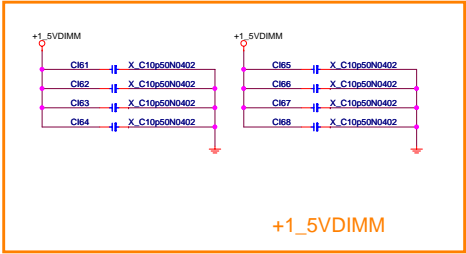
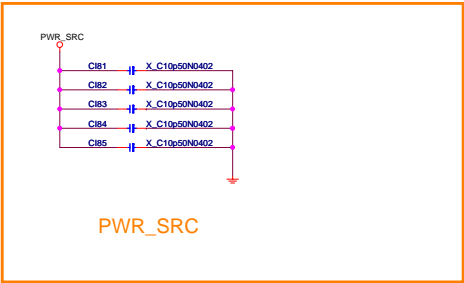
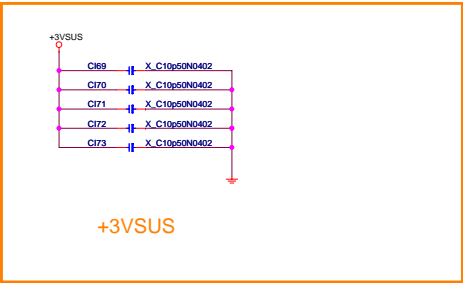
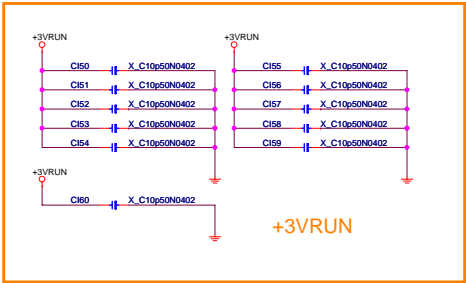


50 ohm



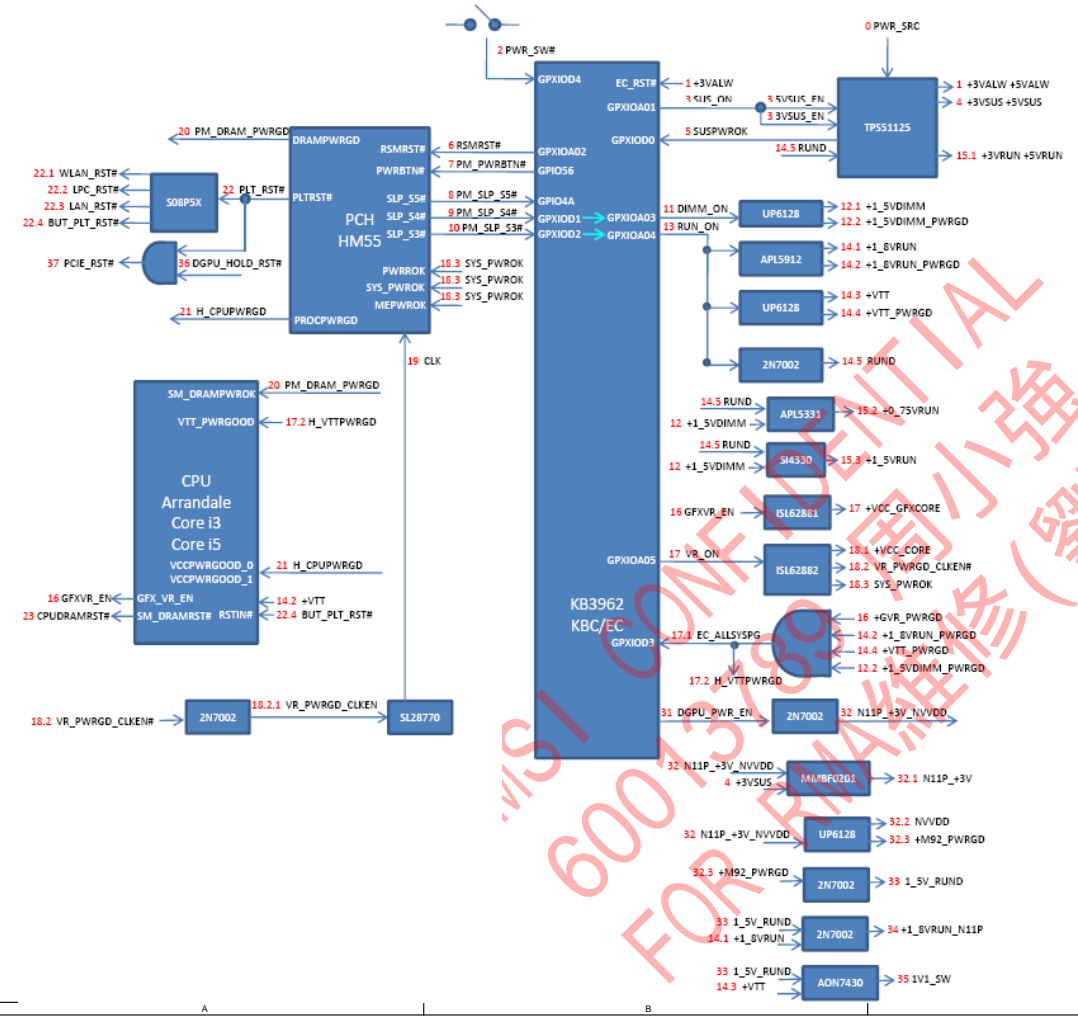
2010/02/01 Reserve for EMI request



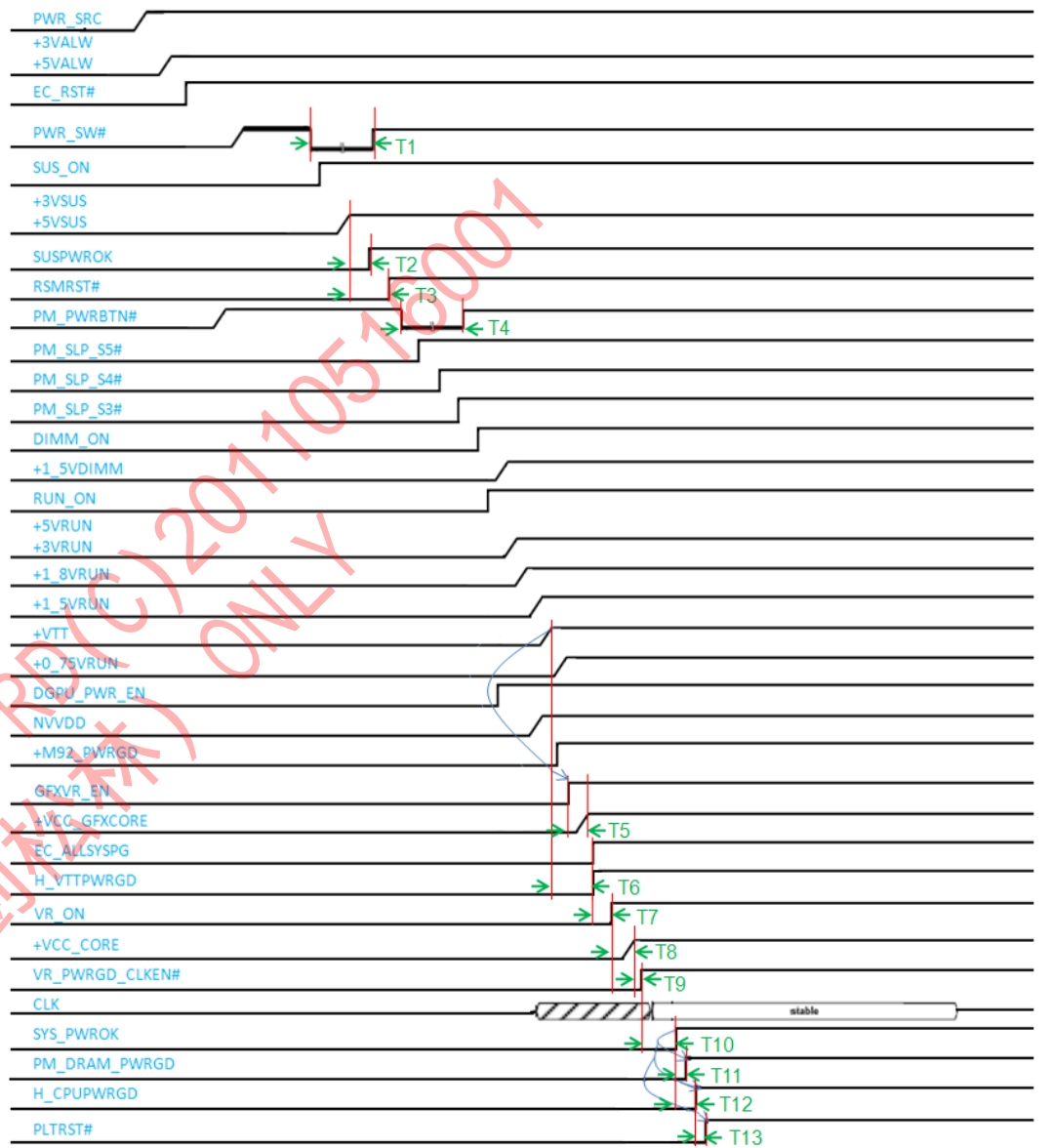


2010/02/01 Reserve power by pass capacity for EMI request

Label	Min	Max	Units	Description
T1	150		ms	
T2	2	2.5	ms	The powergood function is activated with 2 ms internal delay after SUSPWROK goes high. If the output voltage becomes within +/-5% of the target value, PGOOD goes high around 2.5 ms after SUSPWROK goes high.
T3	10		ms	Vcc_SUS stable to RSMRST# deassertion.
T4	150		ms	
T5		1	us	CPU will drive Gfx_VR_EN when VTT ramps. Gfx_VR_EN to Gfx_VID stable. Timing set by Processor.
T6		500	ms	VTT stable to VITTPWRGOOD assertion to the processor.
T7	99		ms	ALL_SYS_PWRGD assertion to IMVP_VR_EN. This timing is generated by EC.
T8		3	ms	
T9	10	100	us	
T10	3	20	ms	IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
T11	1		ms	SYS_PWROK/PCH_PWROK assertion to DRAMPWROK assertion. Timing set by PCH.
T12	1		ms	SYS_PWROK/PCH_PWROK assertion to VOCPPWRGOOD/VOCPPWRGOOD_1 assertion. Timing set by PCH.
T13	1		ms	VOCPPWRGOOD_0/VOCPPWRGOOD_1 assertion to PLTRST# deassertion.

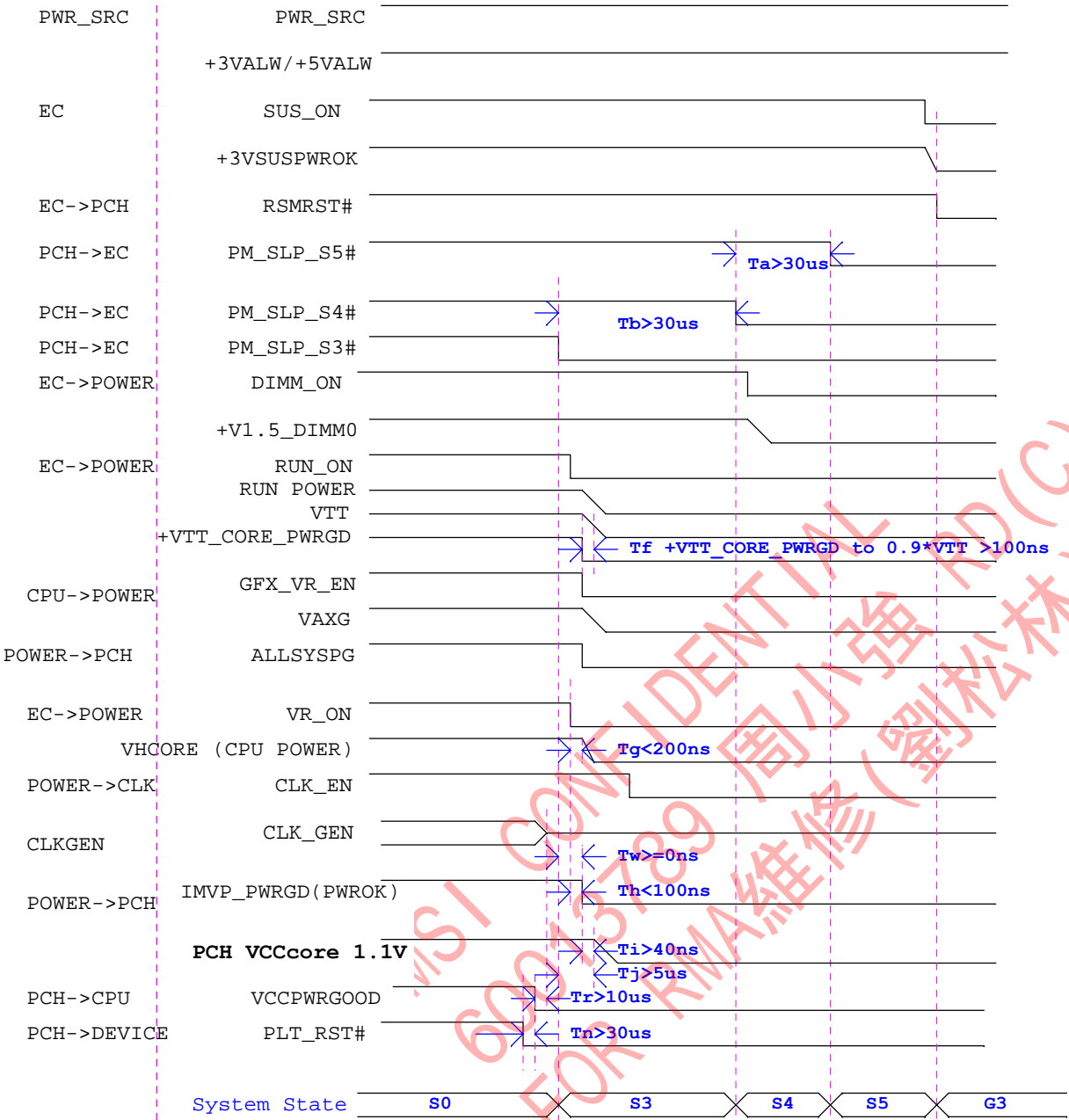


Calpella System Power on Sequence DC mode





Power down Sequence DC mode S0 to G3





0A NOTE

2009/12/25

- 1.Change Aduio codec form ALC 888 to ALC 269
- 2.Change LAN Chip from RTL 8111DL to RTL 8111EL

2009/12/29

- 1.For Power team request change the power page(P.38~P.43) to same the 16G1
- 2. Page 21 For Layout request reversal the PCH Azialia arry resistor sequency
- 3. Page 22 For Layout request reversal the PCH SMBus arry resistor sequency
- 4. Page 5 Remove PROCHOT# line, Add test point
- 5. Page 45 ADD VOL+\_SW,VOL\_-\_SW,EC0\_SW,HIQ\_SW,TURBO\_SW

2009/12/30

- 1.For Card reader ENE suggestion add 4.7K ohm pull hi to 3V
- 2. P40,P41,P43 delete Nvidia Venthura power desgin

2009/12/31

- 1. Page 38 Change power connector

2010/01/03

- 1. Page 46 Add TP board
- 2. Page 12, 13 modify off page symbol
- 3. Page 35 follow reference schematic remover 3 capacity

2010/01/04

- 1. Page 35 follow reference schematic add 10K pull low
- 2. Page 44 Remove NV I/O 1.8V
- 3. Page 45 follow ENE suggestion change the capacity to 20P

2010/01/05

- 1. Page 3 Change decoupling capacity from X5R to X7R
- 2. Page 31 Add CRT HSYNC &VSYN level shift
- 3. Page 47 remove HDD LED MOSFET

2010/01/07

- 1. Page 38 For EMI request change capacity from 22p to 10p

2010/01/08

- 1. Page 43 For OC reserve adjust voltage schemaitc
- 2. Page 44 For OC reserve adjust voltage schemaitc

2010/01/12

- 1.Page 38 follow Realtek suggestion modify PD# schematic
- 2.Page 39 Remove power schematic for power team request
- 3.Page 40 Chagne R1230 from 174K(0603) to 178K(0402) for power team request
- 4. Page 38 remove OD schematic for Realtek suggestion
- 5. Page 38 Add and change pull hi resistor to 4.7K
- 6. Page 38 Change power connector same the 16G1

2010/01/13

- 1. Page 32 Change keyboard Connector for 87 Keys
- 2. Page 33 Change ESATA CONN PN

2010/01/14

- 1. Page 47 Change TP Pin define for multi finger
- 2. Page 42 reserve GFX VID pull & low resistor
- 3. Page 11 Nvidia Recommend R200 isn't stuff
- 4. Page 12 Change pull low resistor value form 1% to 5%
- 5. Page 13 Change pull low resistor value form 1% to 5%
- 6. Page 18 Change pull low resistor value form 1% to 5%
- 7. Page 19 Change pull low resistor value form 1% to 5%
- 8. Page 19 Nvidia recommend change R103 & R104 value from 10K to 2.2K ohm
- 9. Page 19 Nvidia recommend reserve I2CS for thermal sensor
- 10. Page 40 For adjust power sequence modify schematic

2010/01/15

- 1. Page 9.10 Change reserve capacity value form 2.2uF to 10uF
- 2. Page 9.10 Remove the x-copper, add verf\_ca resistor 10K\*2

2010/01/18

- 1. Page 19 Add reserve pull hi and pull low resistor for Nvidia recommend
- 2. Page 32 & 46 Change Connector from 16 pin to 14 pin

2010/01/19

- 1. Page 36 Fro EMI request change reserve capacity location
- 2. Page 39 Fro power team request swap the MOSFET location
- 3. Page 32 Change the smith trigger unit at schematic
- 4. Page 43 Change smith trigger part reference
- 5. Page 34 Reserve Level shift IC pin 38 add 2.2K pull low
- 6. Page 48 Change CPU+PCH Screw to holes\_r276d185s

2010/01/20

- 1. Page 33 For Me request change H.D.D connector P/N
- 2. Page 19 Add GPIO 5 & 6 Pull hi & Pull low resistor for Nvidia request
- 3. Page 48 Change PCH-Stand-off PN E2B-1431010-L63

2010/01/21

- 1. Page 07 Change 0R to X-copper
- 2. Page 08 Change 0R to X-copper
- 3. Page 9 Stuff C77 & Stuff Vref CA resister
- 4. Page 9 Stuff C52 & Stuff Vref CA resister
- 5. Page 11 Change C155,C256,C272,C196,C268 to no stuff
- 6. Page 12 Change C413 to no stuff and Add C572
- 7. Page 18 Change C166,C173,C470 to no stuff
- 8. Page 21 remove resistor to TP point save for layout space
- 9. Page 31 Change Pin define and remove reserve component for layout space save and save cost (common used 1471 LVDS cable)
- 10. Page 24 used LVDS cable same the 1471, can save other LVDS write
- 11. Page 38 Add capacity for voltage stable
- 12. Page 33 Remove component to save layout space

2010/01/22

- 1. Page 35 Add Q33,R45,C573,U35 for LAN ECO
- 2. Page 11 Change 0R to x-copper tosave component
- 3. Page 32 Change array capacity to save layout space
- 4. Page 46 For ID request Add LED \*4
- 5. Page 41 For power team request modify capacity value from 470uF 10 68uF
- 6. Page 45 modify screw size for ME
- 7. Page 23 modify resistor 1K to 10K
- 8. Page 31 modify R369,R359 to stuff
- 9. Page 24 remove component to save layout space
- 10. Page 40 Reserve capacity for fine tune timing
- 11. Page 30 modify FSA pull high to 10KR
- 12. Page 30 modify Crystal(Y6) for ME height limit
- 13. Page 32 Key board follow 1471 pin define

2010/01/25

- 1. Page 32 Rechange array capacity to capacity
- 2. Page 45 Add location holes for ME
- 3. Page 46 Add location holes for ME
- 4. Page 47 Add location holes for ME
- 5. Page 21 BIOS PN pending change to M31-25L3203-M24
- 6. Page 13 Resistor PN peding change to R11-402AT12-W08
- 7. Page 19 Resistor PN peding Change to R11-402AT12-W08
- 8. Page 28 Bead PN pending change to L01-1006084-T19
- 9. Page 48 For EMI suggestion change MH8 GND to AGND

2010/01/26

- 1. Page 48 modify stand-off for ME request
- 2. Page 12 reserve pull hi resistor for Nvidia request
- 3. Page 13 reserve pull hi resistor for Nvidia request
- 4. Page 47 Add TP CLK & DATA pull hi resistor
- 4. Page 37 for ME request modify the MDC connecotr PN

2010/01/27

- 1. Page 48 modify stand-off for ME request
- 2. Page 25 for layout request swap RN6 pin define
- 3. Page 37 & 45 connector pin define
- 4. Page 47 reserve capacity for EMI request

2010/01/28

- 1. Page 48 modify screw for EMI request

2010/01/29

- 1. Page 34 Add resistor for TI suggestion

2010/02/01

- 1. Page 47 Swap TP connector pin define for ME cable
- 2. Page 45 no stuff USB EMI common choke
- 3. Page 37 no stuff USB EMI common choke
- 4. Page 45 Reserve capacity for EMI request
- 5. Page 47 Reserve capacity for EMI request
- 6. Page 47 Reserve capacity for EMI request
- 7. Page 49 Reserve power by pass capacity for EMI request
- 8. Page 48 Reserve GND Pad for EMI request
- 9. Page 41 For high frequency issue modify 68uF to 100uF

2010/02/02

- 1. Page 41 Change net and add net name for vendor suggestion
- 2. Page 41 Reserve 330uF capacity for high frequency issue


2010/02/03

- 1. Page 37 USB Pin 2 & Pin 3 Pin 2 swap
- 2. Page 45 Delete USB MEC pin to GND
- 3. Page 45 Delete USB MEC pin to GND

2010/02/09

Note for 0B CN4,VGA1,CN2,USB1,MICA1,LOUT1 fot 產線製程改爲60階,0B需改回原本階層

Begging to now total adding components :81

 MICRO-STAR INT'L CO.,LTD.			
File			
0A NOTE			
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2010/02/09

Note 1 CN4,VGA1,CN2,USB1,MICA1,LOUT1 for SMTchange to 60 status,remind 0B version must change to default status

Note 2. remind 0B version msut change 14.318MHz & 25MHz crystal to mainstream source

2010/03/03

1.Page 35 modify CHOKE1 form 2.2uH to 4.7uH for Realtek request

2010/03/07

1.Page 31 Add CRT fuse for safety request

1.Page 38 Change C569,C416,L22,C416,C411 ,C529,C530 t0 stuff

2010/03/11

1.Page 37 modify USB connector PN:N53-04M0580-AF2

2.Page 32 remove TP baord pull hi resistor to mainboard

2010/03/11

1.Page 13 modify R190 value form 60R to 40R for NV suggestion

2.Page 37 for ME modify USB1 Connector PN to N53-04M0580-AF2

2010/03/16

1.Page 19 modify R157,R160 value form 40.2R to 40.2K

2.Page 40 Add NV 1.1V timing delay schematic

2010/03/21

1.Page 18 remove JNCA2 at 0B version

2.Page 18 modify C179 to no stuff at 0B versionn

2010/03/22

1.Page 30 modify Y6 PN:D04-0100900-F07  
c load value form 22p to 20p

2010/03/22

1.Page 22 Resever Wimax solution

2.Page 42 Resever for EMI request

2010/03/24

1.Page 39 modify PL1 PN to L04-1007340-M26

2.Page 43 modify PR21 PN to R11-1132T12-W08

3.Page 44 modify PC107 stuff

4.Page 43 modify R265 to stuff

5.Page 44 modify PR105 to 4.75K

6.Page 44 modify PR106 to 1.5K

2010/03/25

1.Page 48 modify Mini PCI-E Solt for ME request

1.Page 48 modify Mini PCI-E Stand off for ME request

2010/03/26

1.Page 42 modify PR 93 value to 4.87K ohm

2.Page 48 modify Mini PCI-E Stand off for ME request

3.Page 35 reserve 0.1uF \*4 for EMI

4.Page 35 modify Xcopper to 0R

5.Page 41 modify PR120,Pr128 to 1.82KR

6.Page 41 modify PR125,PR49 to 2.49KR

7.Page 41 modify PR133 to 3.3KR

8.Page 41 modify PR131 to 7.87 KR

9.Page 41 modify PR136 to 63.4KR

10.Page 41 modify PC125 value to 0.068uF

11.Page 40 modify PR10value to 30.9K

12.Page 38 for DEPOP function stuff DEPOP schematic

13.Page 43 modify PR14,PR15 value to 1K

14.Page 46 modify DB4 & DB6 color to Amber  
modify DB2,DB3,DB7,DB8 to no stuff for ID request

2010/03/29

1.Page 37 modify USB switch IC to ANPEC

2.Page 45 modify USB switch IC to ANPEC

3.Page 21 remove BIOS socket modify to ROM

4.Page 31 modify L3,L4,L5 to indutor 120nH for EMI suggestion

5.Page 31 modify C92,C104,C108 to stuff

6.Page 46 Add Launch board Mylar for ME

7.Page 47 Add TP board Mylar for ME

2010/03/30


1.Page 36 For EMI request to stuff C100

2.Page 32 For EMI request to stuff KB capacity(CI40、CI48、CI39、CI47、CI38、CI46、CI37、CI45、CI36、CI44、CI35、CI43、CI34、CI42、CI33、CI41)


3.Page 32 For EMI request to stuff ER1 & EC1

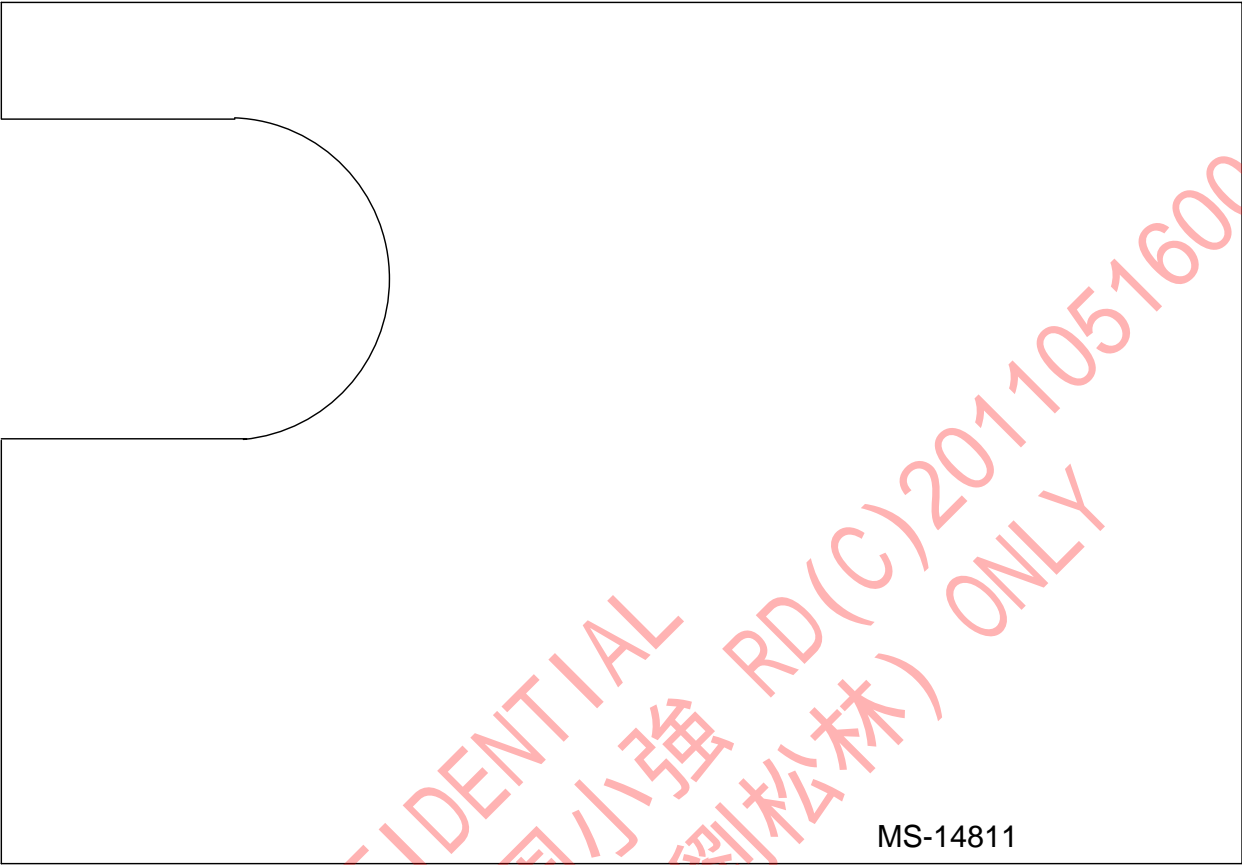
4.Page 30 For EMI request to stuff CI8

5.Page 25 For EMI request to stuff CI9,C110,CI49


		MICRO-STAR INT'L CO.,LTD.	
Title			
0B NOTE			
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